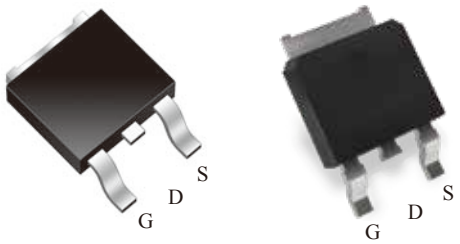
General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for DC/DC Converter, Synchronous Rectification and a load switch in battery powered applications.

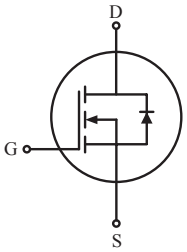
MAIN PARAMETER

V_{DSS}	100	V
$R_{DS(ON)}$ (Max)@V_{GS}=10V	22	mΩ
I_D	32	A

DPAK(1) DPAK(3)



PIN CONNECTION



FEATURES

- Split Gate Trench Technology
- Ultra low on-resistance
- Ultra Low gate charge (typ. Qg=17.0nC)
- Periodic avalanche rated
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC

  Ideal for high-frequency switching and synchronous rectification

MAXIMUM RATING(Tc=25 ℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	@T_C=25 ℃	I_D	32	A
	@T_C=100℃		20	
	Pulsed (Note 1)	I_{DP}	120*	
Single Pulsed Avalanche Energy	(Note 2)	E_{AS}	39	mJ
Repetitive Avalanche Energy	(Note 1)	E_{AR}	2.1	mJ
Peak Diode Recovery dv/dt	(Note 3)	dv/dt	4.5	V/ns
Drain Power Dissipation	Tc=25 ℃	P_D	39	W
	Derate above 25℃		0.31	W/℃
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55 ~ 150	℃
Thermal Characteristics				
Thermal Resistance, Junction-to-Case		R_{thJC}	3.1	℃/W
Thermal Resistance, Junction-to-Ambient		R_{thJA}	110	℃/W

* : Drain current limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (Tc=25 ℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA, V_{GS}=0V	100	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_j$	I_D=250 μA, Referenced to 25℃	-	0.05	-	V/℃
Drain Cut-off Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V,	-	-	10	μA
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250 μA	2.0	-	4.0	V
Gate Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=16A	-	17	22	mΩ
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V, I_D=32A V_{GS}=10V (Note4,5)	-	17.0	-	nC
Gate-Source Charge	Q_{gs}		-	4.2	-	
Gate-Drain Charge	Q_{gd}		-	4.1	-	
Turn-on Delay time	$t_{d(on)}$	V_{DD}=50V I_D=32A R_G=25Ω (Note4,5)	-	18	-	ns
Turn-on Rise time	t_r		-	22	-	
Turn-off Delay time	$t_{d(off)}$		-	46	-	
Turn-off Fall time	t_f		-	17	-	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	1060	-	pF
Output Capacitance	C_{oss}		-	390	-	
Reverse Transfer Capacitance	C_{rss}		-	39	-	
Source-Drain Diode Ratings						
Continuous Source Current	I_S	V_{GS}<V_{th}	-	-	28	A
Pulsed Source Current	I_{SP}		-	-	112	
Diode Forward Voltage	V_{SD}	I_S=28A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_S=32A, V_{GS}=0V, dIs/dt=100A/ μs	-	51	-	ns
Reverse Recovery Charge	Q_{rr}		-	0.11	-	μC

Note 1) Repetivity rating : Pulse width limited by junction temperature.

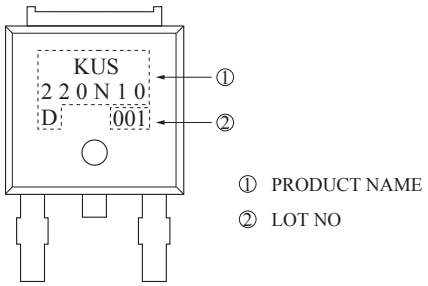
Note 2) L = 43μH, I_S=32A, V_{DD}=50V, R_G=25 Ω, Starting T_j=25℃.

Note 3) $I_S \leq$32A, $V_{DD} \leq BV_{DSS}$, Starting T_j =25℃.

Note 4) Pulse Test : Pulse width ≤300 μs, Duty Cycle ≤2%.

Note 5) Essentially independent of operating temperature.

MARKING



① PRODUCT NAME

② LOT NO

Fig1. I_D - V_{DS} - Ⅰ

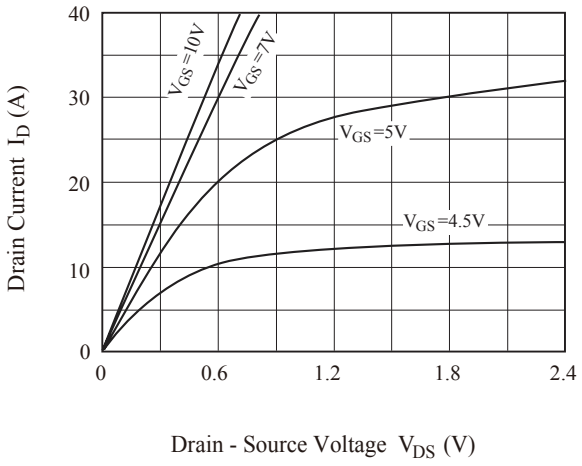


Fig2. I_D - V_{DS} - Ⅱ

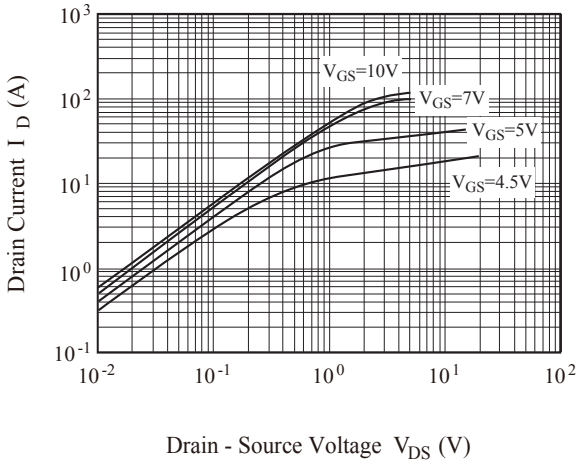


Fig3. I_D - V_{GS}

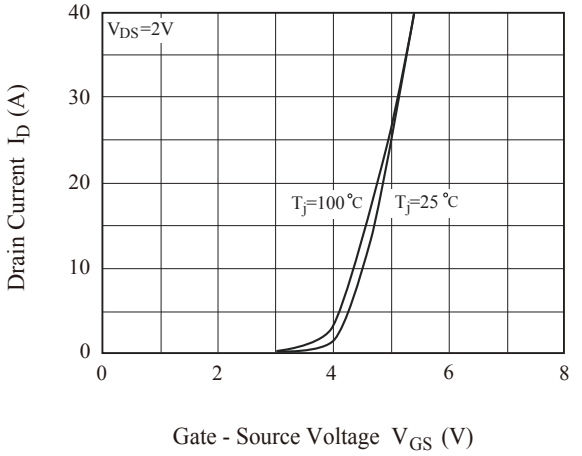


Fig4. $R_{DS(ON)}$ - I_D

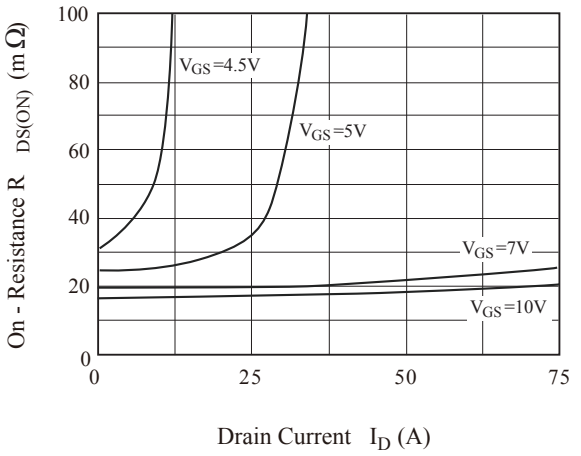


Fig5. $R_{DS(ON)}$ - V_{GS}

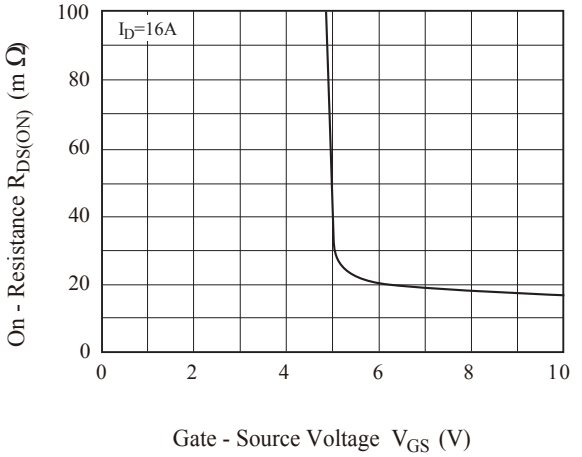


Fig6. $R_{DS(ON)}$ - T_j

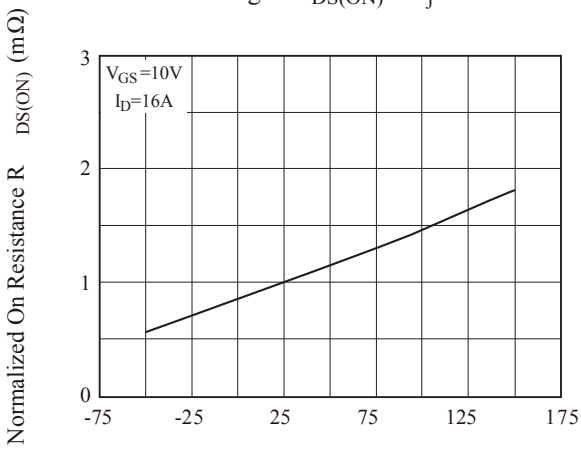


Fig7. BV_{DSS} - T_j

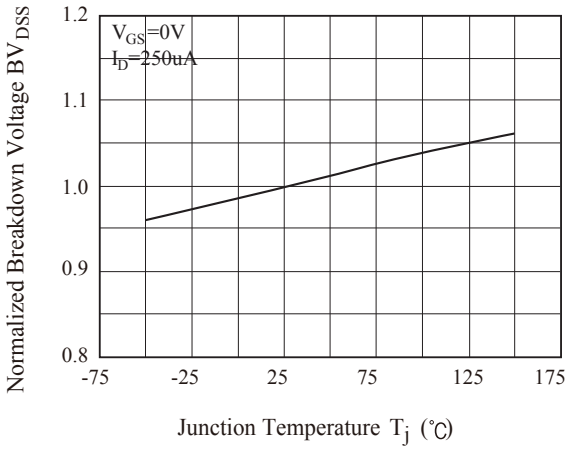


Fig8. V_{th}- T_j

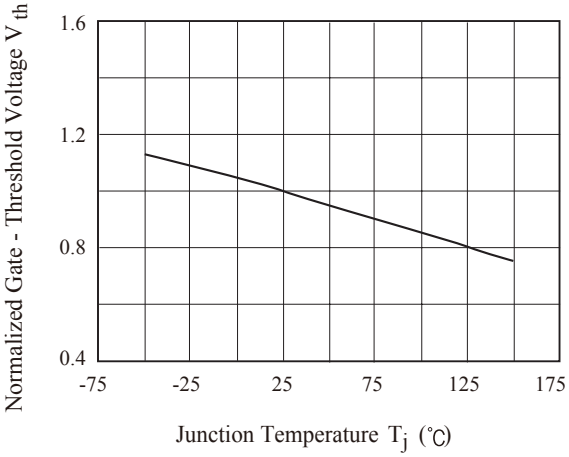


Fig 9. I_S - V_{SD} - Ⅰ

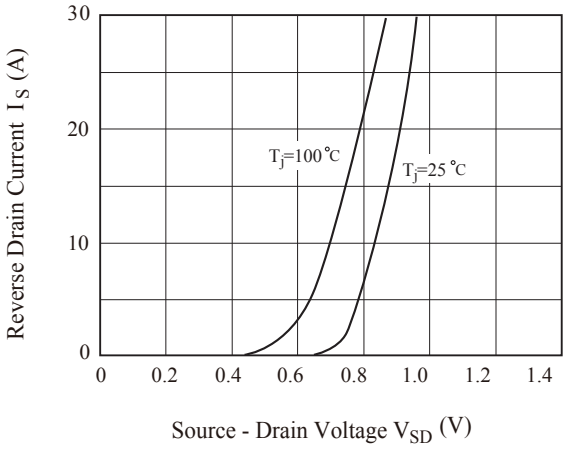


Fig10. I_S - V_{SD} - Ⅱ

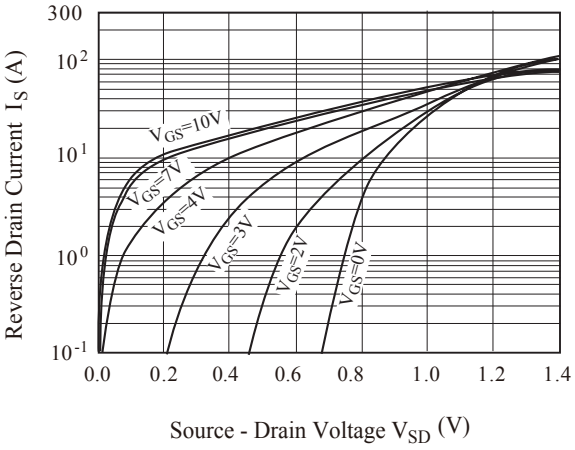


Fig11. C - V_{DS}

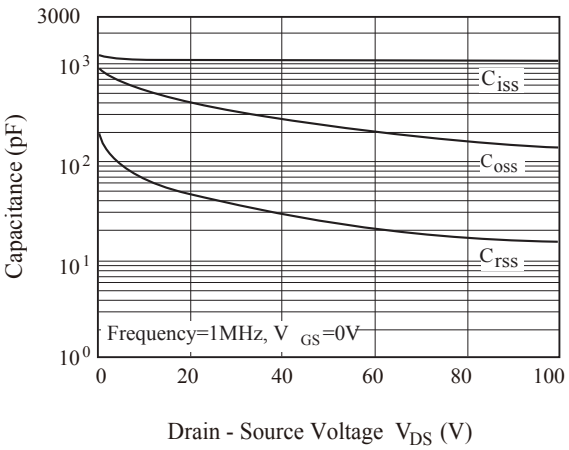


Fig12. Q_g- V_{GS}

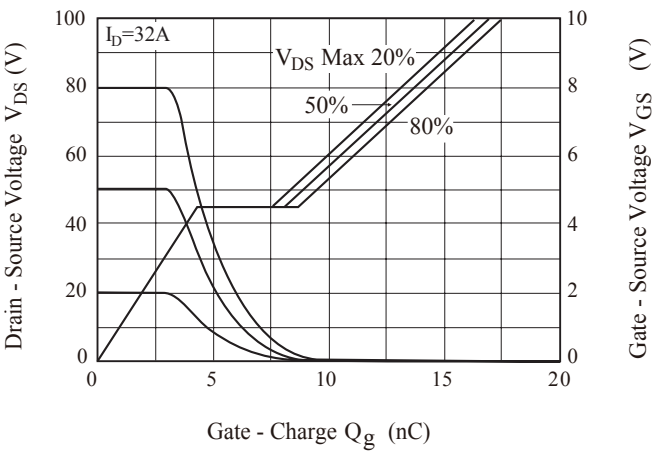


Fig13. I_D - T_j

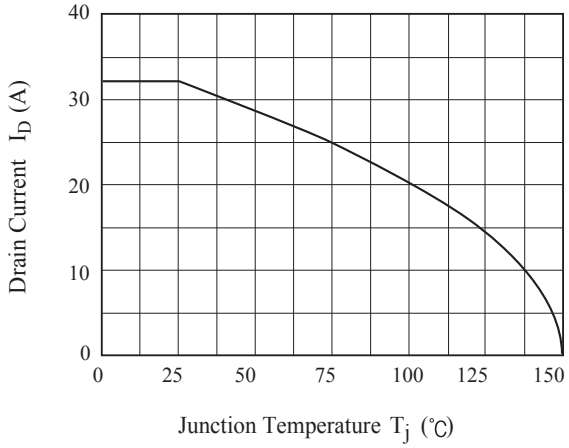


Fig14. P_{tot} - T_C

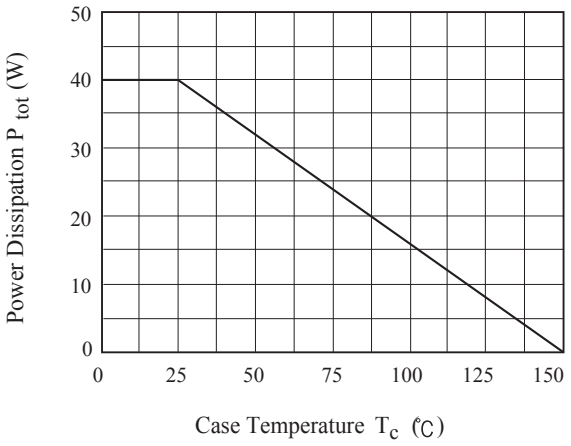


Fig15. S/W Time - I_D

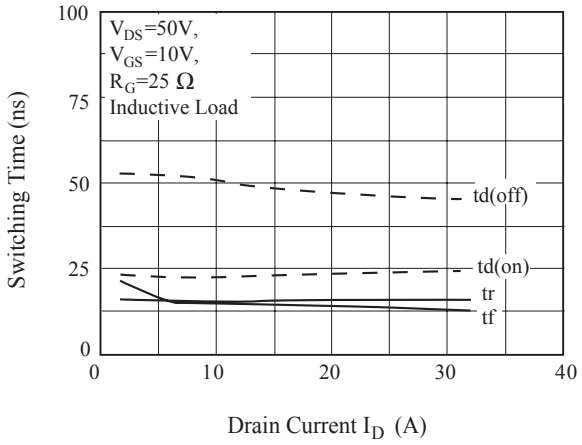


Fig16. S/W Loss - I_D

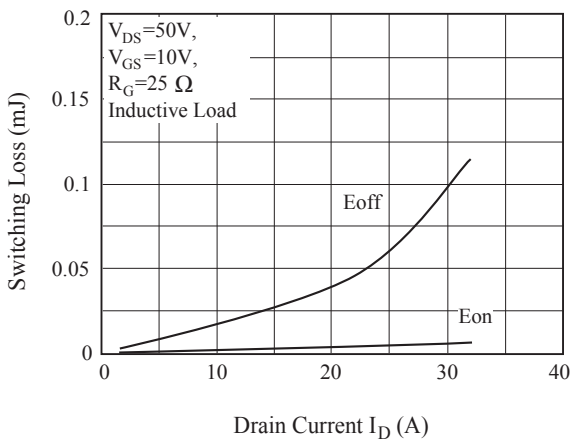


Fig17. S/W Time - R_G

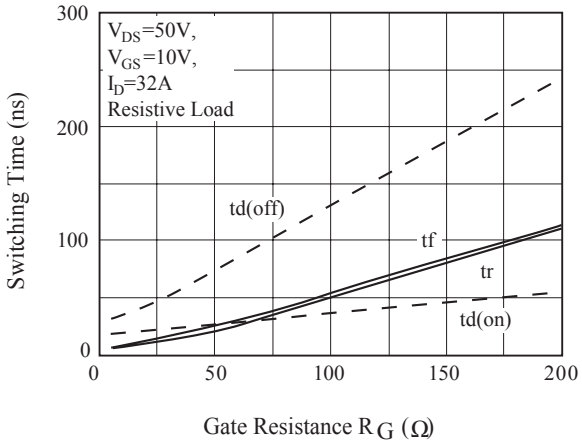


Fig18. S/W Loss - R_G

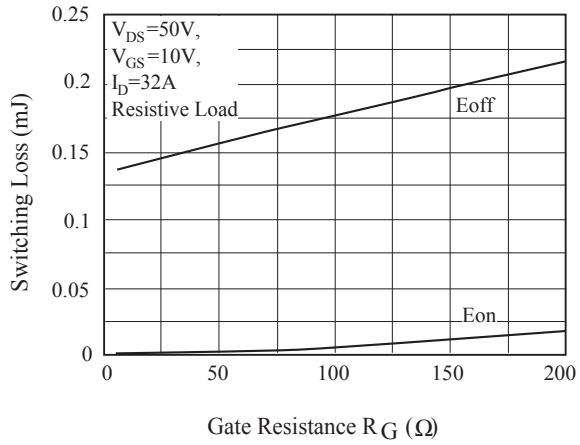


Fig 19. Safe Operation Area

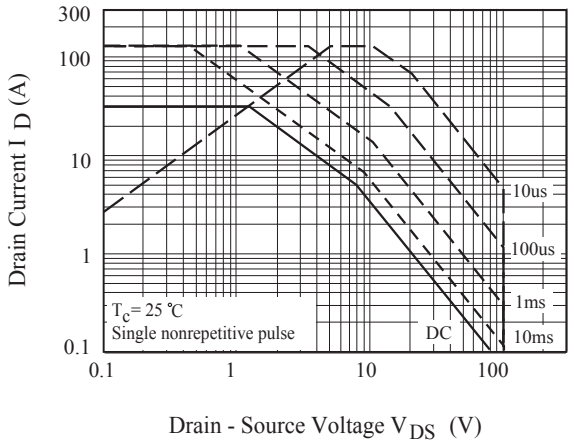


Fig20. Transient Thermal Response Curve
(Junction - Case)

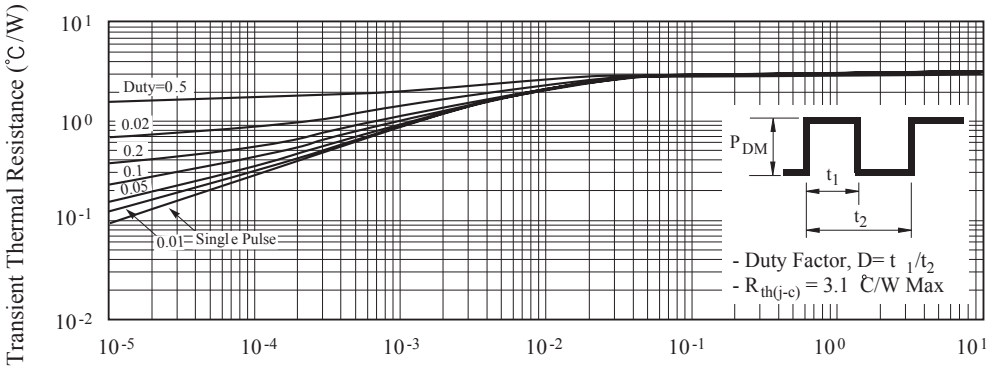


Fig21. Transient Thermal Response Curve
(Junction - Ambient)

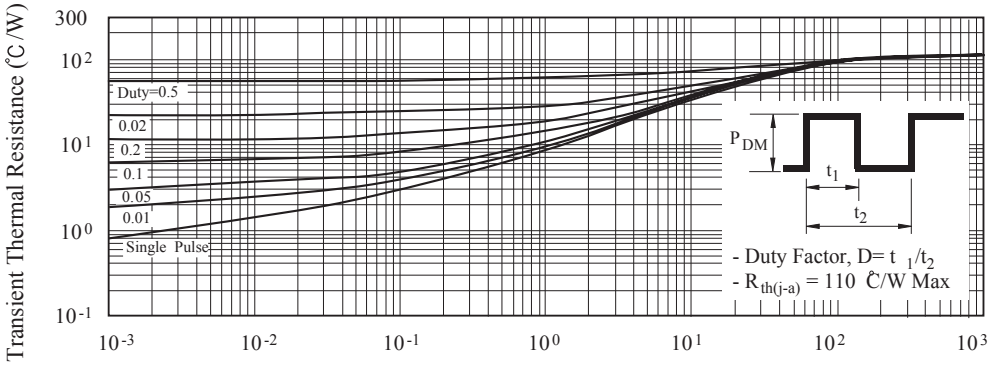
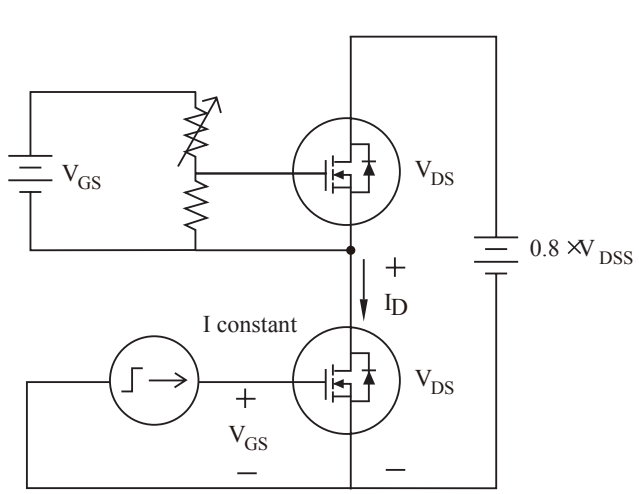


Fig22. Gate Charge



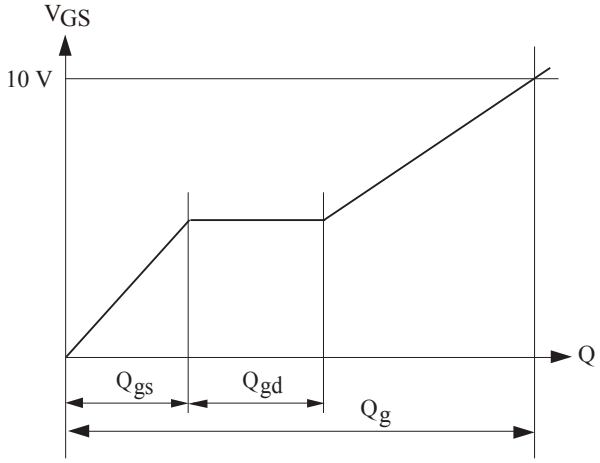
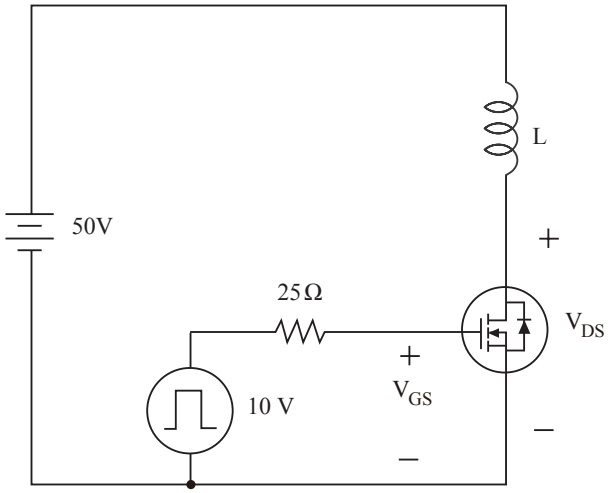


Fig23. Single Pulsed Avalanche Energy



$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

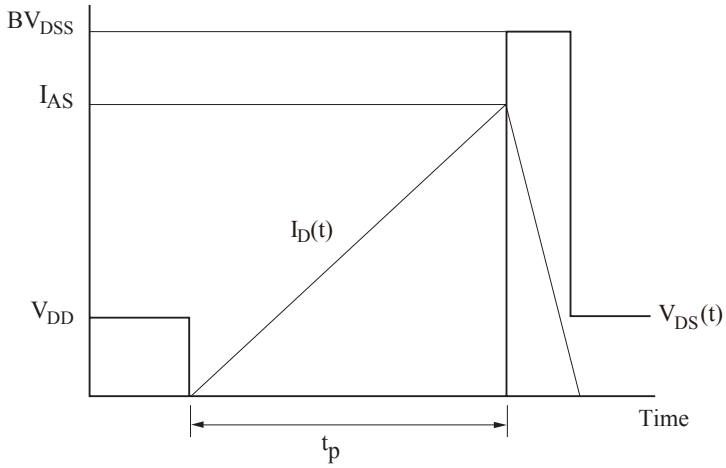
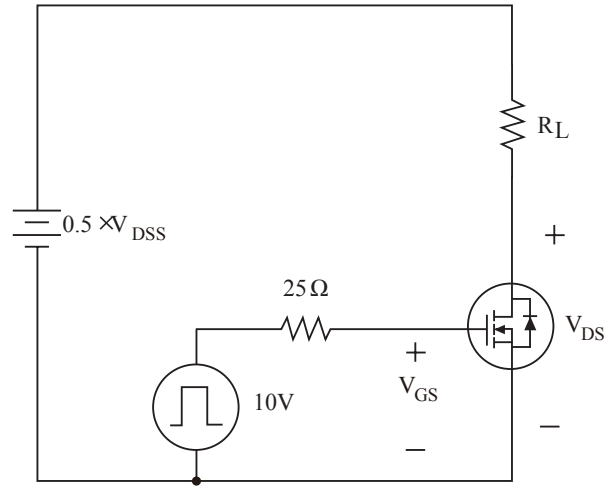


Fig24. Resistive Load Switching



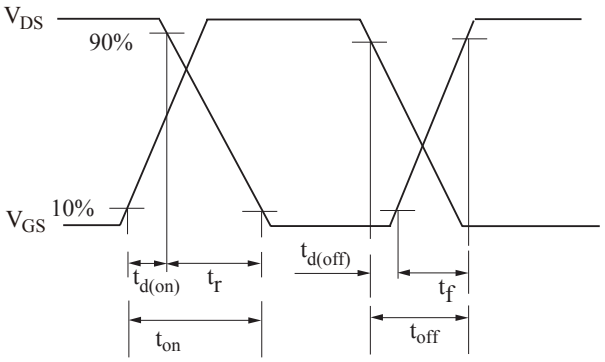
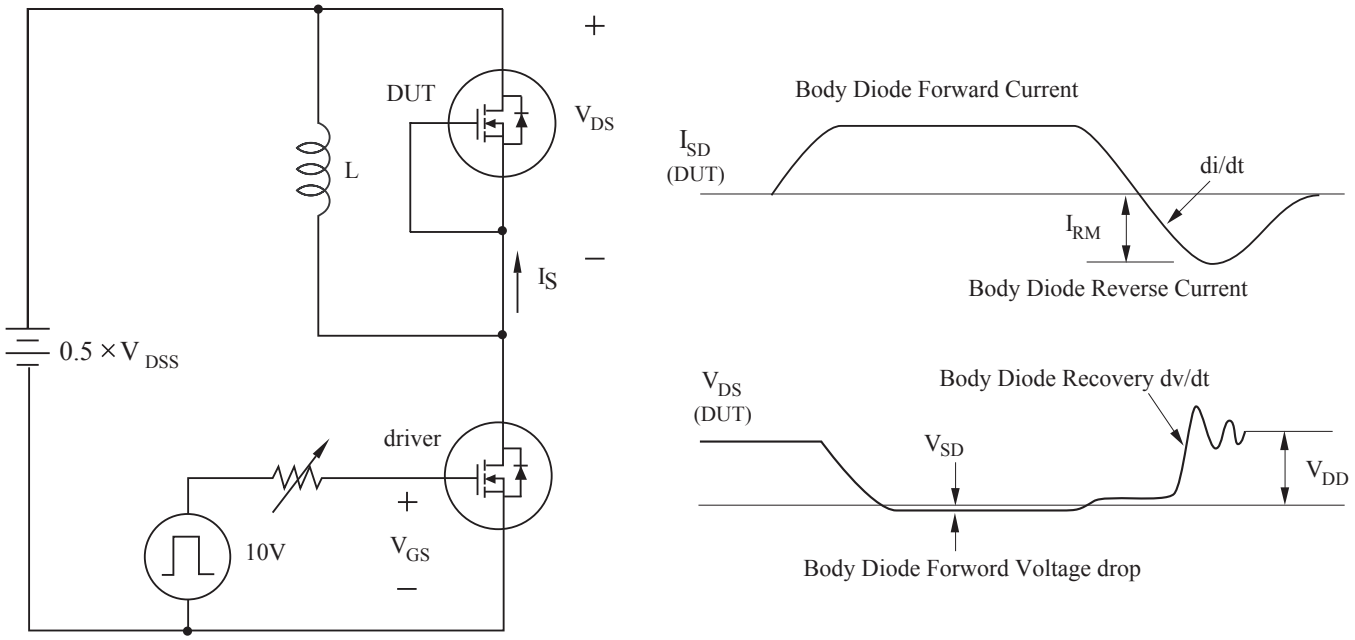
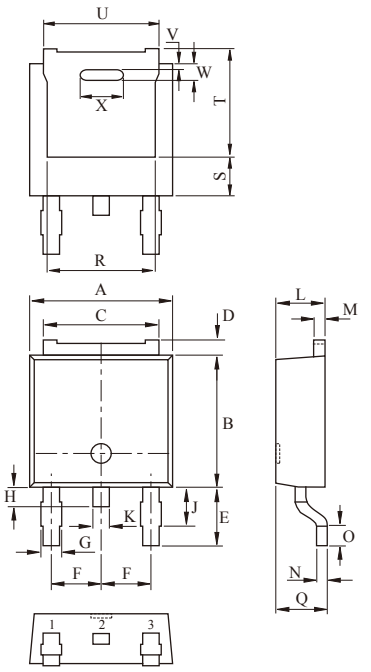


Fig25. Source - Drain Diode Reverse Recovery and dv /dt

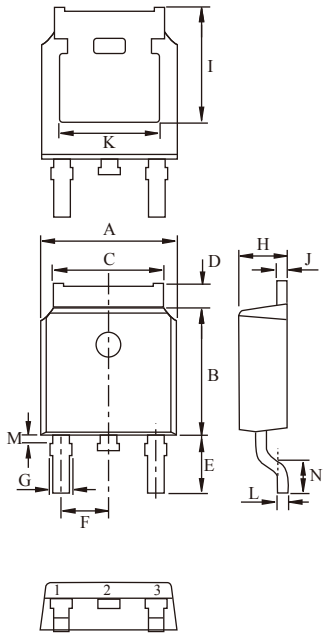


PACKAGE OUTLINE



DIM	MILLIMETERS
A	6.60 ± 0.20
B	6.10±0.20
C	5.34 ±0.30
D	0.70±0.20
E	2.70 ± 0.15
F	2.30±0.10
G	0.96 MAX
H	0.90 MAX
J	1.80±0.20
K	0.76±0.20
L	2.30±0.10
M	0.50 ± 0.10
N	0.50±0.10
O	0.70 MIN
Q	2.4±0.2
R	5.0±0.2
S	1.75±0.3
T	5.0±0.3
U	5.34±0.3
V	0.27±0.05
W	0.77±0.1
X	2.0±0.1

DPAK (1)



DIM	MILLIMETERS
A	6.60±0.1
B	6.1±0.1
C	5.33±0.2
D	1.1±0.2
E	2.90 REF
F	2.286±0.1
G	0.9 Max.
H	2.3±0.1
I	5.25 Min
J	0.5±0.1
K	4.70 Min
L	0.508 BSC
M	0.75 Max
N	1.5±0.2

DPAK (3)