KU310N10D

N-ch Trench MOS FET

General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for DC/DC Converter, Synchronous Rectification and a load switch in battery powered applications

FEATURES

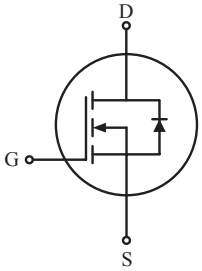
- V_{DSS}= 100V, I_D= 27A
- Drain-Source ON Resistance :
  $R_{DS(ON)}$=31mΩ(Max.) @V_{GS} = 10V
- Suffix **U** : Qualified to AEC-Q101.
  ex) KU310N10D-RTF/H**U**

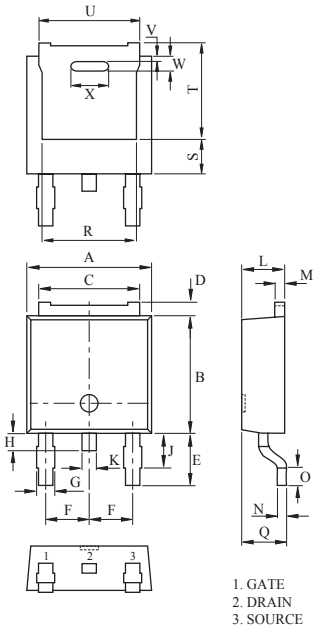
MAXIMUM RATING (Tc=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	@T_C=25℃	I_D	27	A
	@T_C=100℃		17	
	Pulsed (Note1)	I_{DP}	110*	
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	60	mJ
Repetitive Avalanche Energy (Note 1)		E_{AR}	2.3	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Drain Power Dissipation	Tc=25℃	P_D	52	W
	Derate above 25℃		0.42	W/℃
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55 ~ 150	℃
Thermal Characteristics				
Thermal Resistance, Junction-to-Case		R_{thJC}	2.4	℃/W
Thermal Resistance, Junction-to-Ambient		R_{thJA}	110	℃/W

* : Drain current limited by maximum junction temperature.

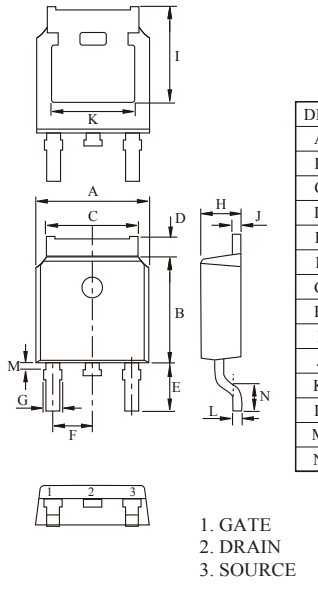
PIN CONNECTION





DIM	MILLIMETERS
A	6.60±0.20
B	6.10±0.20
C	5.34±0.30
D	0.70±0.20
E	2.70±0.15
F	2.30±0.10
G	0.96 MAX
H	0.90 MAX
J	1.80±0.20
K	0.76±0.20
L	2.30±0.10
M	0.50±0.10
N	0.50±0.10
O	0.70 MIN
Q	2.4±0.2
R	5.0±0.2
S	1.75±0.3
T	5.0±0.3
U	5.34±0.3
V	0.27±0.05
W	0.77±0.1
X	2.0±0.1

DPAK (1)



DIM	MILLIMETERS
A	6.60±0.1
B	6.1±0.1
C	5.33±0.2
D	1.1±0.2
E	2.90 REF
F	2.286±0.1
G	0.9 Max.
H	2.3±0.1
I	5.25 Min
J	0.5±0.1
K	4.70 Min
L	0.508 BSC
M	0.75 Max
N	1.5±0.2

DPAK (3)

ELECTRICAL CHARACTERISTICS (Tc=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250㎂, V_{GS}=0V	100	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_j$	I_D=5mA, Referenced to 25℃	-	0.10	-	V/℃
Drain Cut-off Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V,	-	-	10	㎂
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250㎂	2.0	-	4.0	V
Gate Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=13.5A	-	25	31	mΩ
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V, I_D=34A V_{GS}=10V (Note4,5)	-	49	-	nC
Gate-Source Charge	Q_{gs}		-	10	-	
Gate-Drain Charge	Q_{gd}		-	14	-	
Turn-on Delay time	$t_{d(on)}$	V_{DD}=50V I_D=34A R_G=25Ω (Note4,5)	-	30	-	ns
Turn-on Rise time	t_r		-	32	-	
Turn-off Delay time	$t_{d(off)}$		-	115	-	
Turn-off Fall time	t_f		-	40	-	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	2230	-	pF
Output Capacitance	C_{oss}		-	170	-	
Reverse Transfer Capacitance	C_{rss}		-	85	-	
Source-Drain Diode Ratings						
Continuous Source Current	I_S	V_{GS}<V_{th}	-	-	34	A
Pulsed Source Current	I_{SP}		-	-	136	
Diode Forward Voltage	V_{SD}	I_S=13.5A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_S=34A, V_{GS}=0V, dIs/dt=300A/㎲	-	53	-	ns
Reverse Recovery Charge	Q_{rr}		-	0.11	-	㎌

Note 1) Repetivity rating : Pulse width limited by junction temperature.

Note 2) L =35㎌, I_S=34A, V_{DD}=80V, R_G=25Ω, Starting T_j=25℃.

Note 3) $I_S \leq$ 34A, dI/dt≤200A/㎲, $V_{DD} \leq BV_{DSS}$, Starting T_j=25℃.

Note 4) Pulse Test : Pulse width ≤ 300㎲, Duty Cycle ≤ 2%.

Note 5) Essentially independent of operating temperature.

Marking

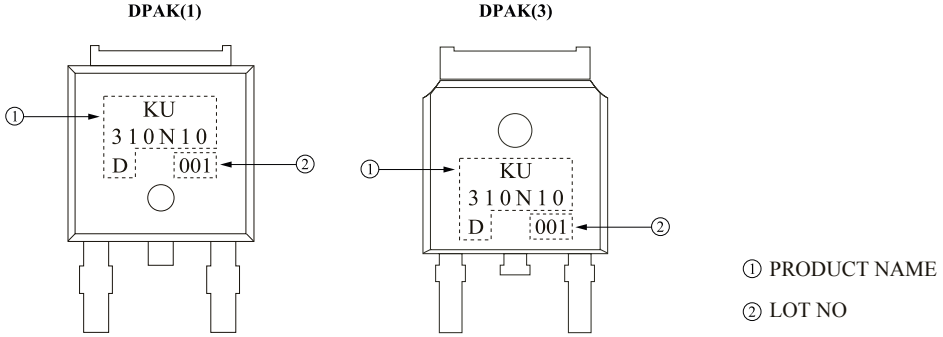


Fig1. I_D - V_{DS}

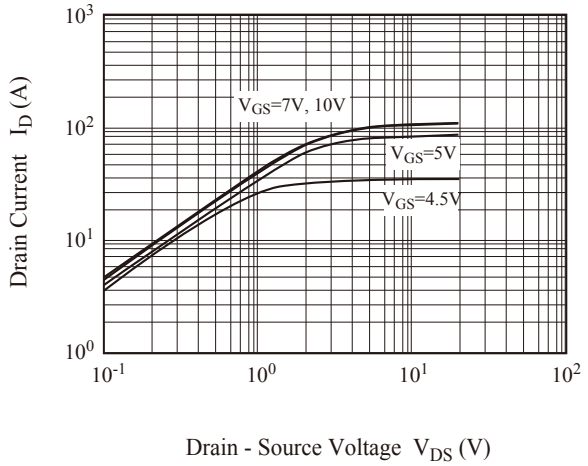


Fig2. I_D - V_{GS}

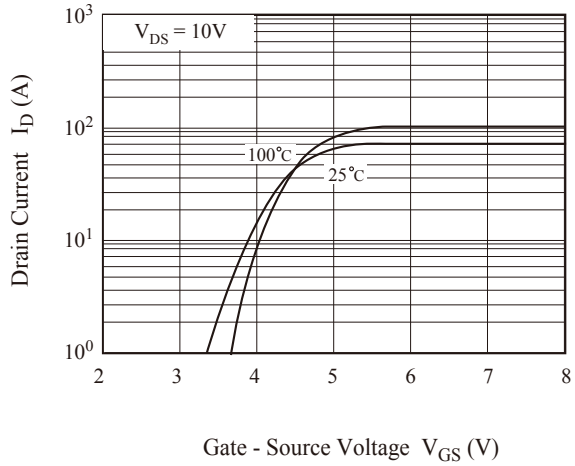


Fig3. BV_{DSS} - T_j

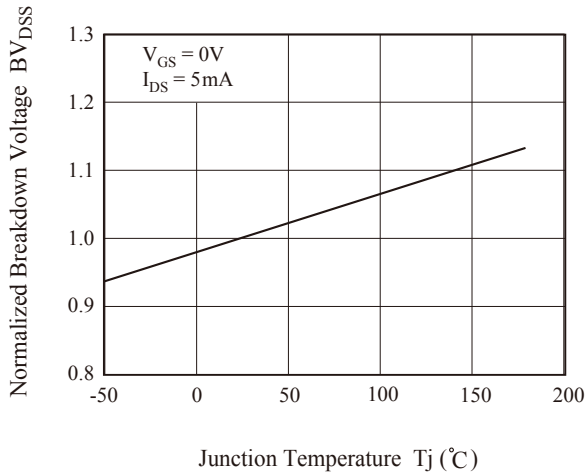


Fig4. $R_{DS(ON)}$ - T_j

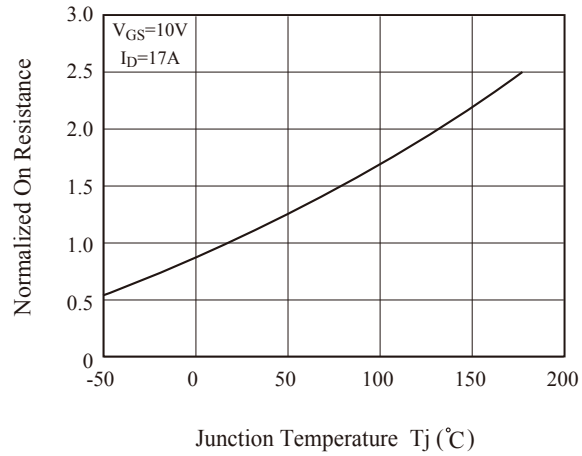


Fig5. V_{th} - T_j

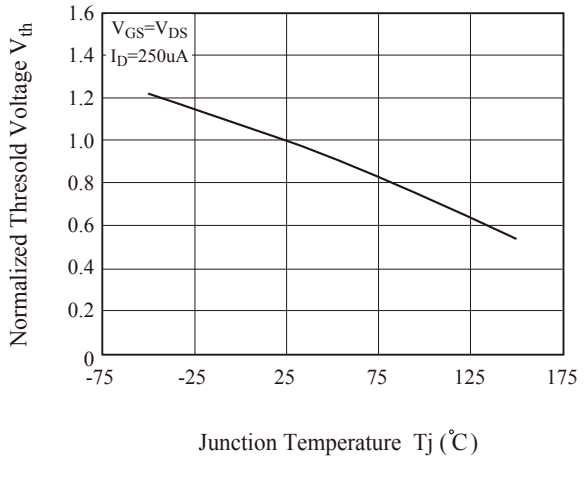


Fig6. I_S - V_{SD} - I

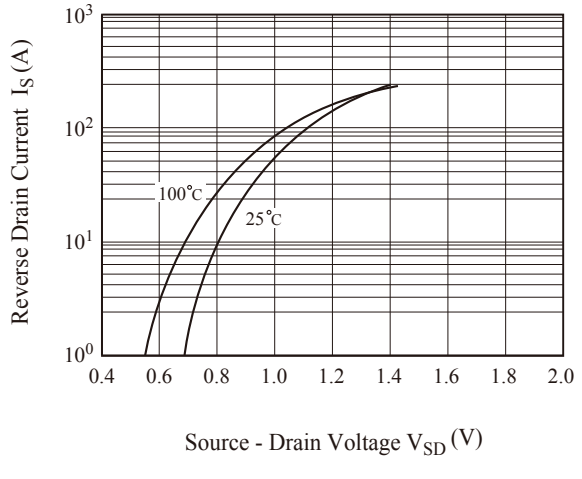


Fig7. I_S - V_{SD} - Ⅱ

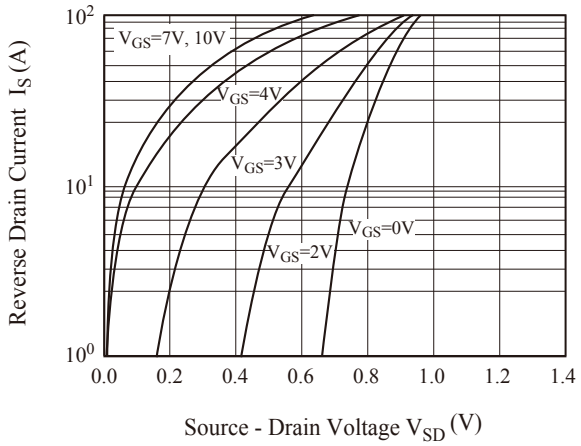


Fig8. $R_{DS(ON)}$ - I_D

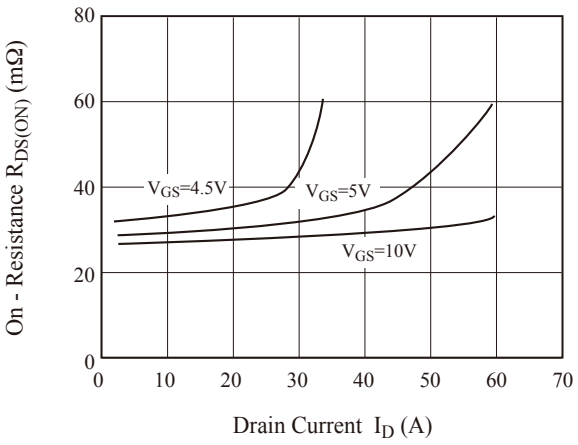


Fig9. I_D- T_j

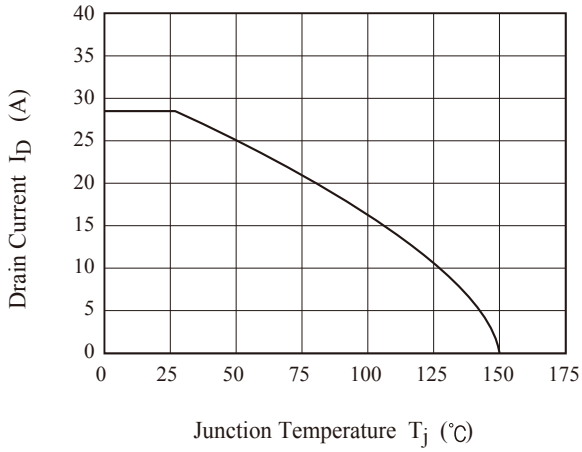


Fig 10. C - V_{DS}

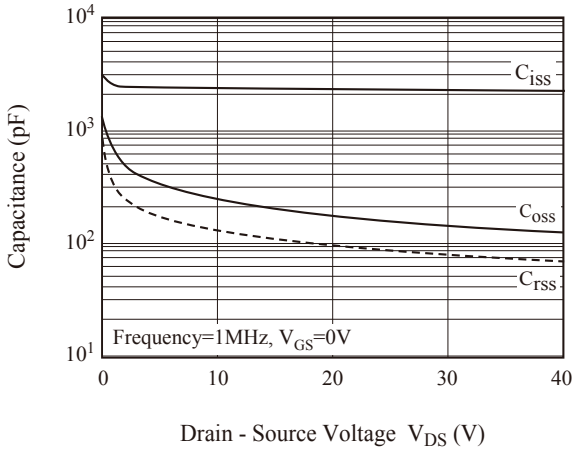


Fig11. Q_g- V_{GS}

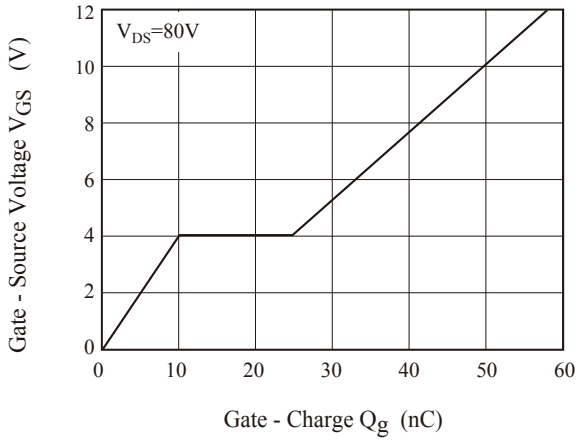


Fig12. Safe Operation Area

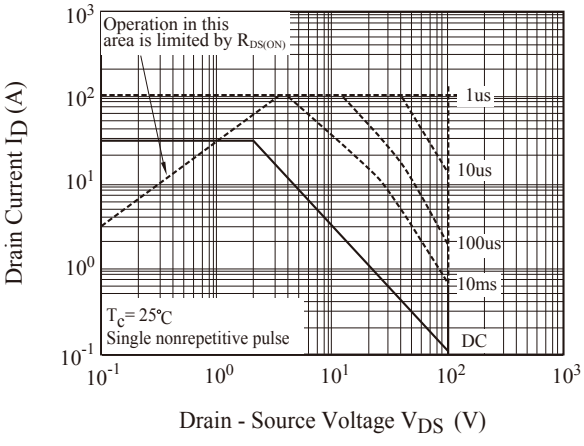


Fig13. Transient Thermal Response Curve

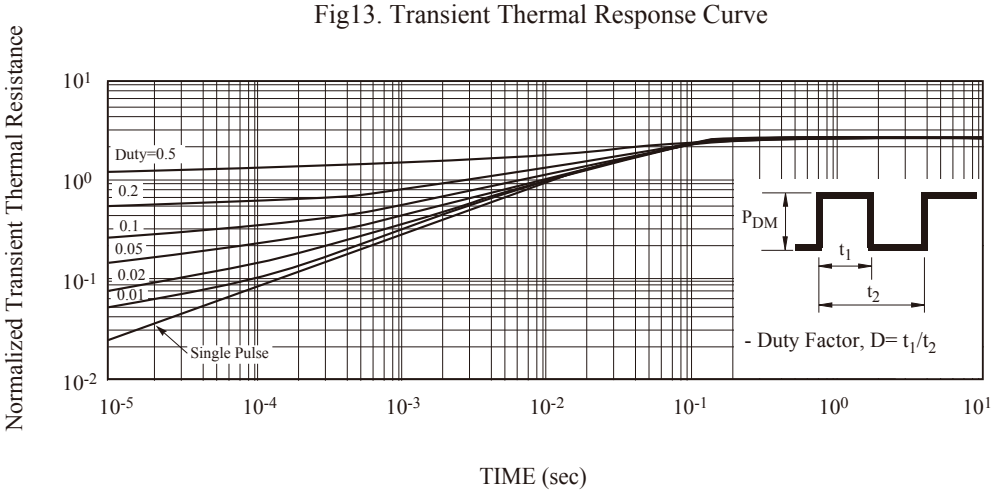


Fig14. Gate Charge

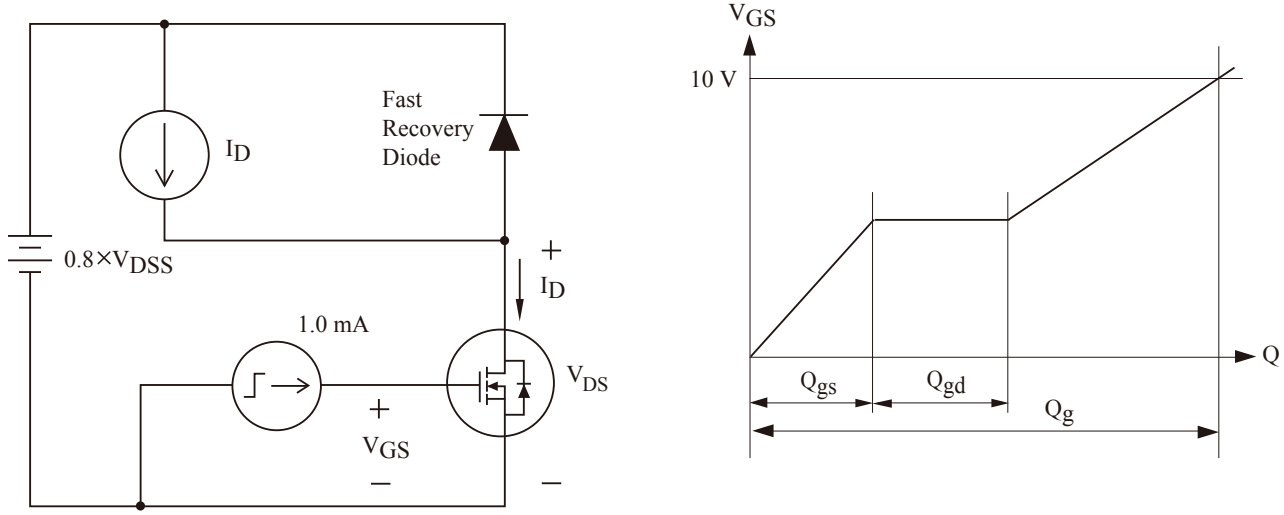


Fig15. Single Pulsed Avalanche Energy

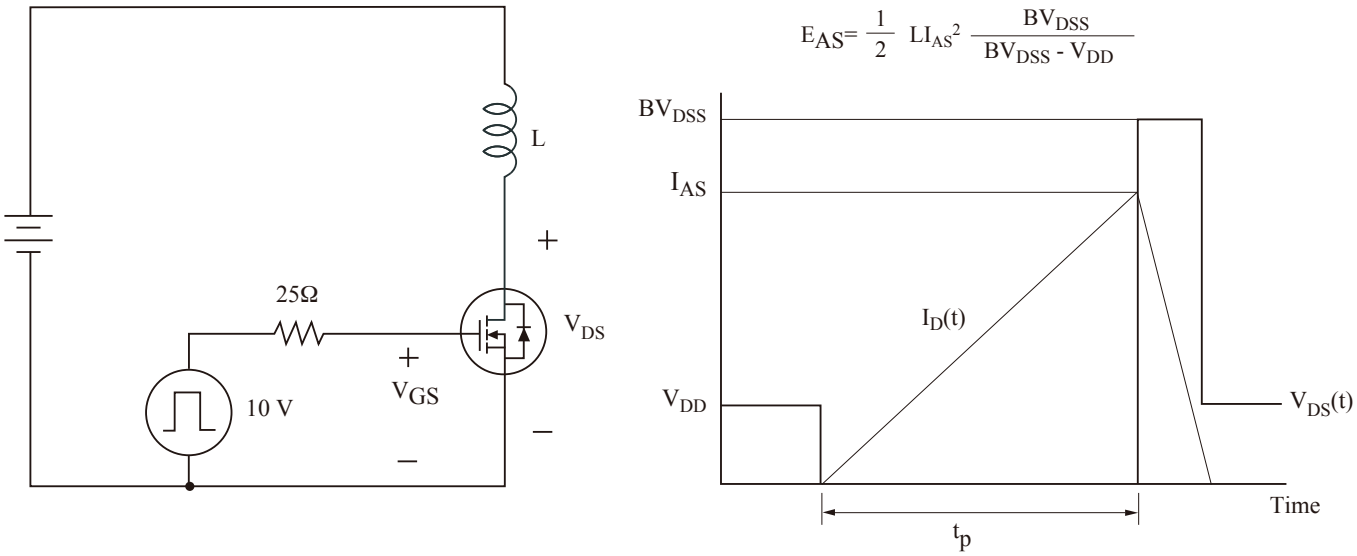


Fig16. Resistive Load Switching

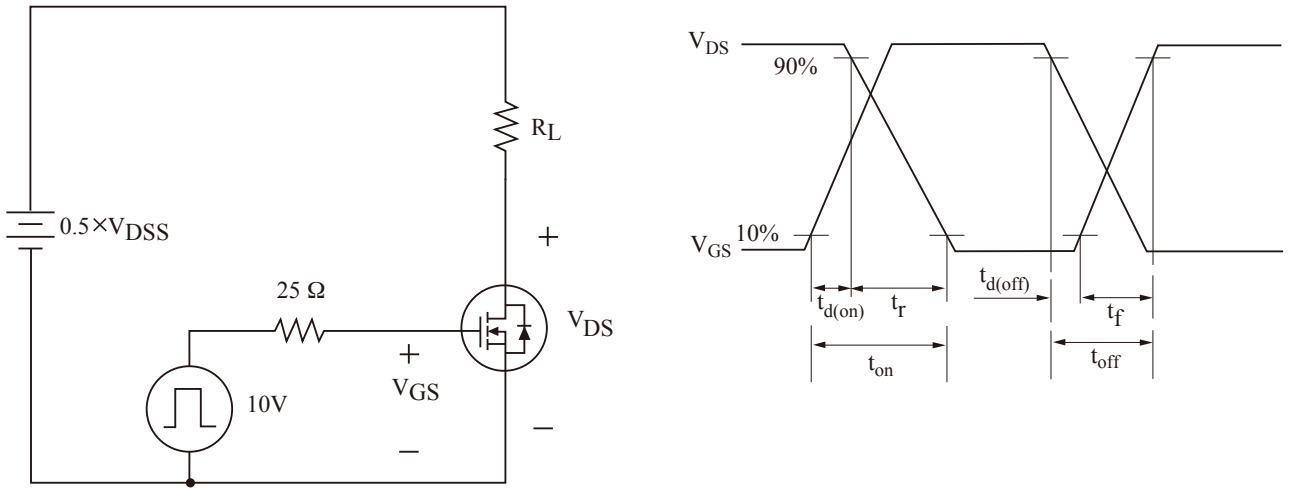


Fig17. Source - Drain Diode Reverse Recovery and dv /dt