General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for DC/DC Converter, Synchronous Rectification and a load switch in battery powered applications

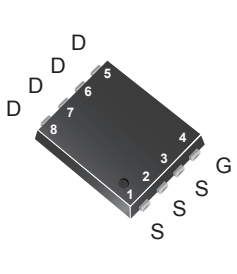
MAIN PARAMETER

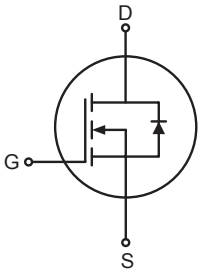
V_{DSS}	100	V
$R_{DS(ON)}$ (Max)@V_{GS}=10V	14	mΩ
I_D	44	A

FEATURES

- Split Gate Trench Technology
- Ultra low on-resistance
- Ultra Low gate charge (typ. Qg=26.0nC)
- Periodic avalanche rated
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC
- Ideal for high-frequency switching and synchronous rectification

PDFN56 **PIN CONNECTION**





MAXIMUM RATING (Tc=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	@T_C=25℃	I_D	44	A
	@T_C=100℃		28	
	Pulsed (Note 1)	I_{DP}	175*	
Single Pulsed Avalanche Energy	(Note 2)	E_{AS}	64	mJ
Repetitive Avalanche Energy	(Note 1)	E_{AR}	2.7	mJ
Peak Diode Recovery dv/dt	(Note 3)	dv/dt	4.5	V/ns
Drain Power Dissipation	Tc=25℃	P_D	49	W
	Derate above 25℃		0.39	W/℃
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55 ~ 150	℃
Thermal Characteristics				
Thermal Resistance, Junction-to-Case		R_{thJC}	2.55	℃/W
Thermal Resistance, Junction-to-Ambient		R_{thJA}	30**	℃/W

* : Drain current limited by maximum junction temperature.

** : Surface mounted on 25 x 25mm FR4 board, t ≤10s

ELECTRICAL CHARACTERISTICS (Tj=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA, V_{GS}=0V	100	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_j$	I_D=250 μA, Referenced to 25℃	-	0.05	-	V/℃
Drain Cut-off Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V,	-	-	10	μA
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250 μA	2.0	-	4.0	V
Gate Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=22A	-	11.3	14	mΩ
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V, I_D=44A V_{GS}=10V (Note4,5)	-	26.0	-	nC
Gate-Source Charge	Q_{gs}		-	7.6	-	
Gate-Drain Charge	Q_{gd}		-	6.0	-	
Turn-on Delay time	$t_{d(on)}$	V_{DD}=50V I_D=44A R_G=25Ω (Note4,5)	-	27	-	ns
Turn-on Rise time	t_r		-	24	-	
Turn-off Delay time	$t_{d(off)}$		-	68	-	
Turn-off Fall time	t_f		-	21	-	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	1700	-	pF
Output Capacitance	C_{oss}		-	580	-	
Reverse Transfer Capacitance	C_{rss}		-	30	-	
Source-Drain Diode Ratings						
Continuous Source Current	I_S	V_{GS}<V_{th}	-	-	35	A
Pulsed Source Current	I_{SP}		-	-	140	
Diode Forward Voltage	V_{SD}	I_S=35A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_S=44A, V_{GS}=0V, dIs/dt=100A/μs	-	56	-	ns
Reverse Recovery Charge	Q_{rr}		-	0.12	-	μC

Note 1) Repetivity rating : Pulse width limited by junction temperature.

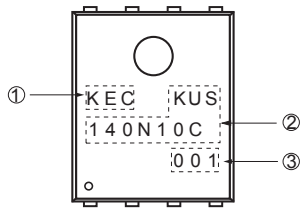
Note 2) L = 38 μH, I_S=44A, V_{DD}=50V, R_G=25Ω, Starting T_j=25℃.

Note 3) $I_S \leq$ 44A, $V_{DD} \leq BV_{DSS}$, Starting T_j=25℃.

Note 4) Pulse Test : Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Note 5) Essentially independent of operating temperature.

MARKING



① KEC LOGO

② PRODUCT NAME

③ LOT NO

Fig1. I_D - V_{DS} - Ⅰ

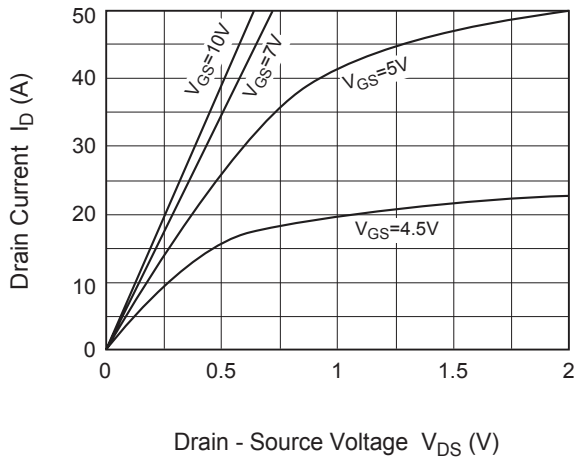


Fig2. I_D - V_{DS} - Ⅱ

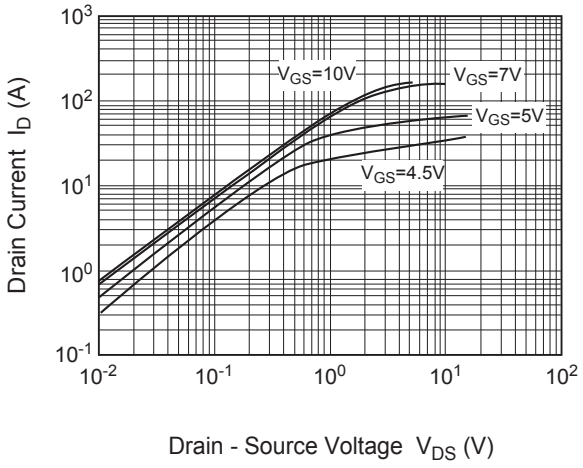


Fig3. I_D - V_{GS}

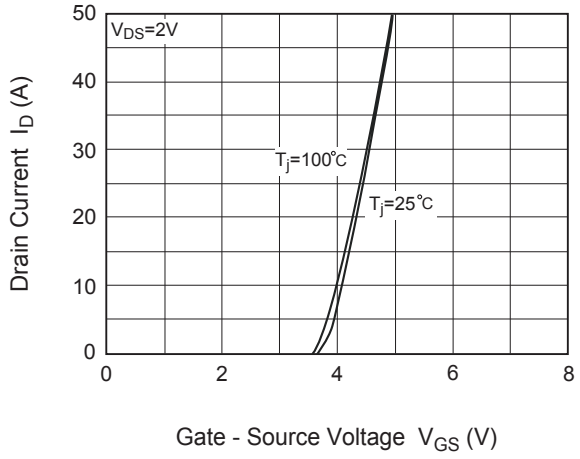


Fig4. $R_{DS(ON)}$ - I_D

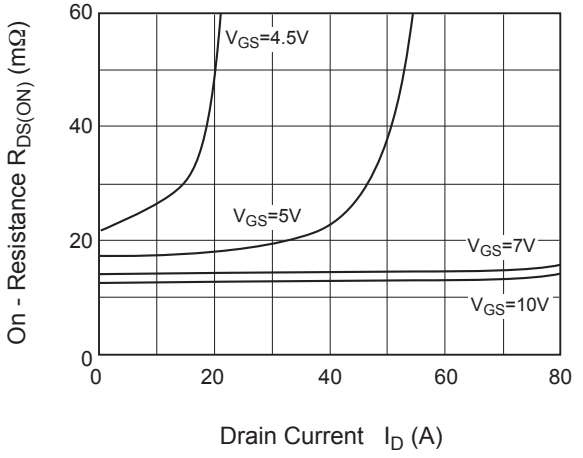


Fig5. $R_{DS(ON)}$ - V_{GS}

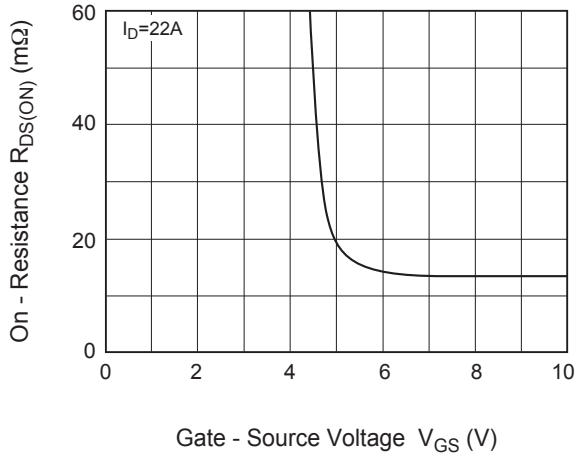


Fig6. $R_{DS(ON)}$ - T_j

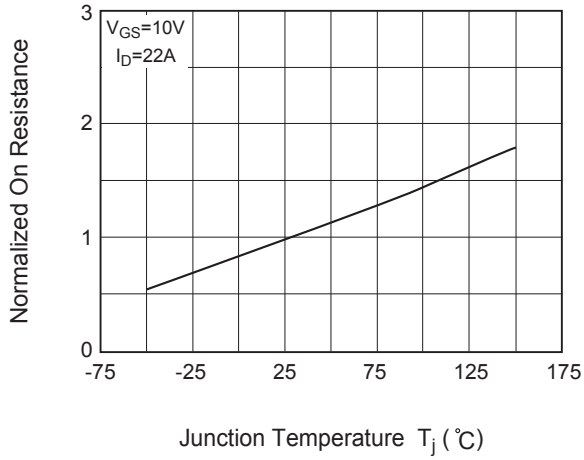


Fig7. BV_{DSS} - T_j

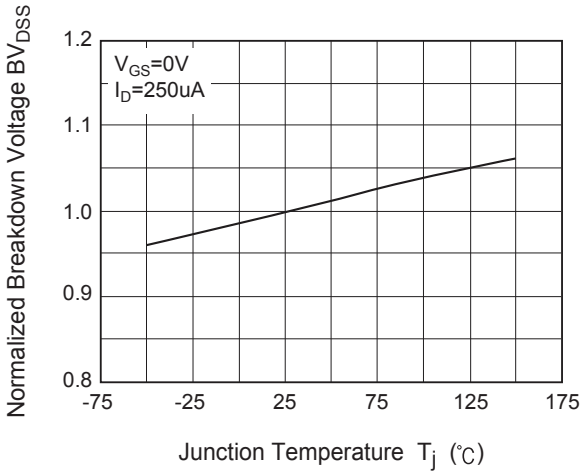


Fig8. V_{th}- T_j

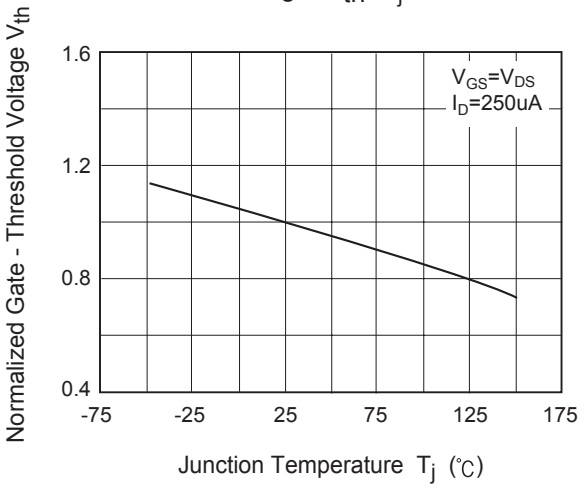


Fig 9. I_S - V_{SD} - Ⅰ

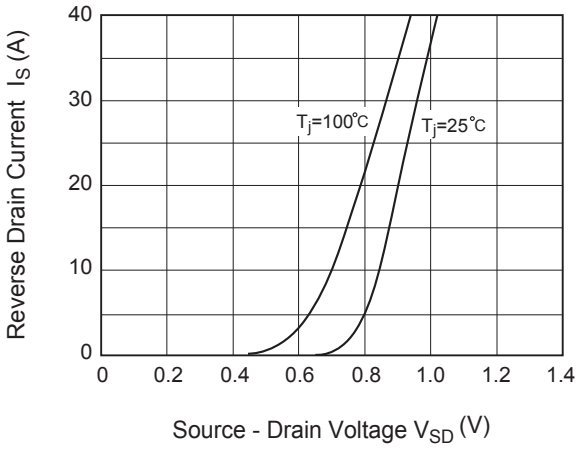


Fig10. I_S - V_{SD} - Ⅱ

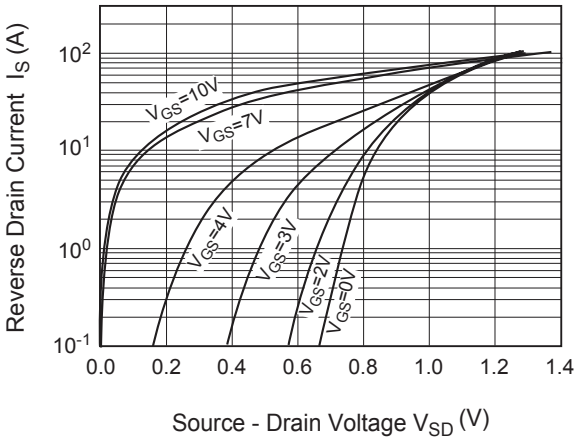


Fig11. C - V_{DS}

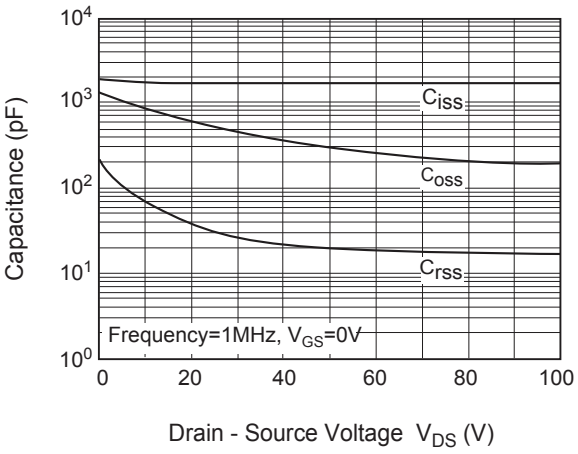


Fig12.Q_g- V_{GS}

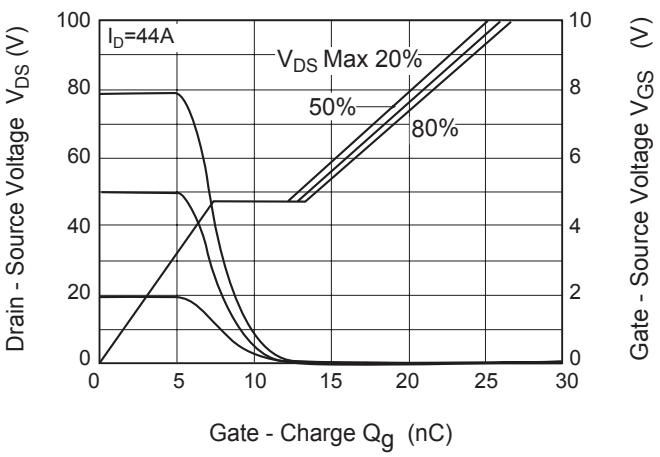


Fig13. I_D - T_C

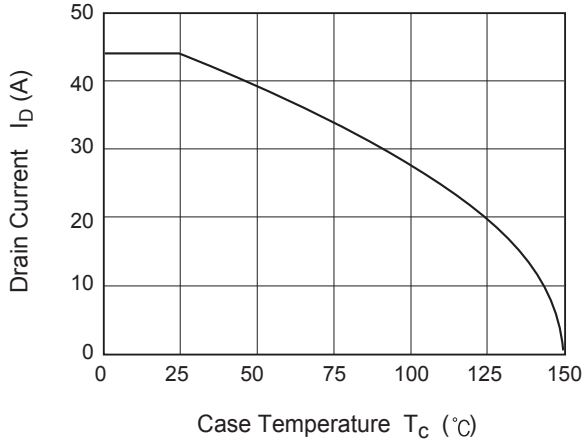


Fig14. P_{tot} - T_C

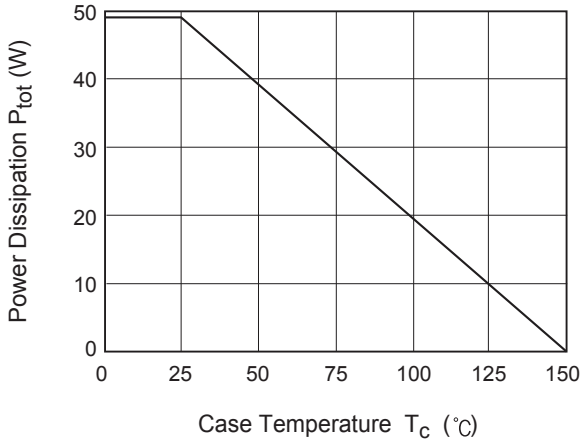


Fig15. t - I_D

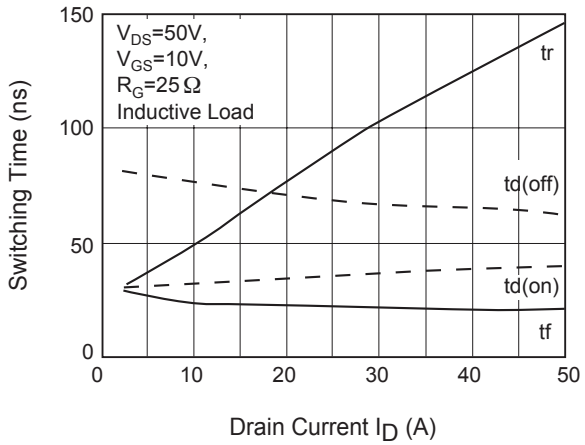


Fig16. S/W Loss - I_D

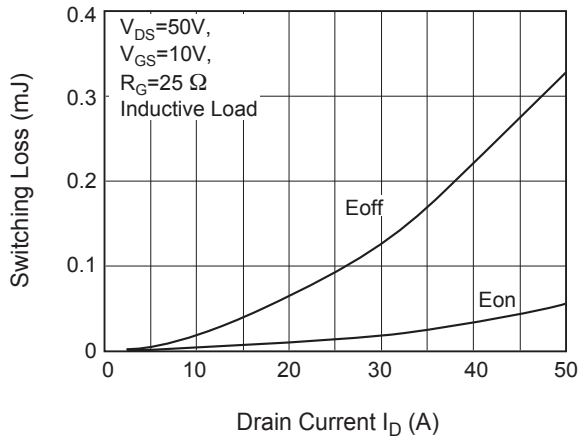


Fig17. S/W Time - R_G

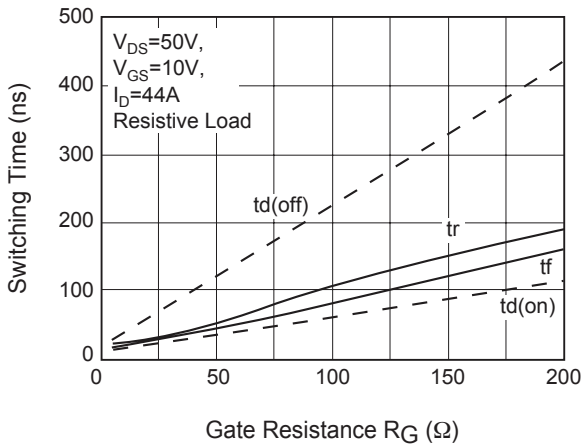


Fig18. S/W Loss - R_G

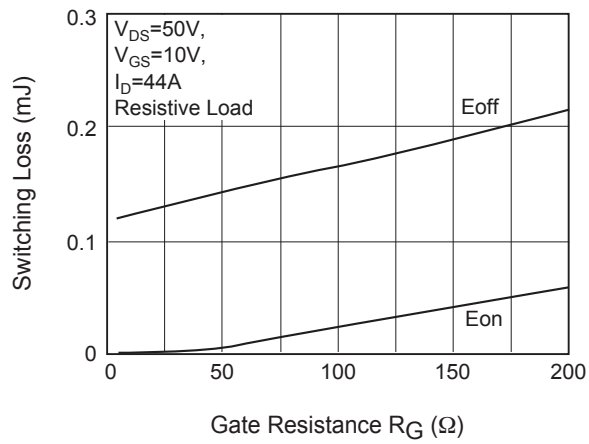


Fig 19. Safe Operation Area

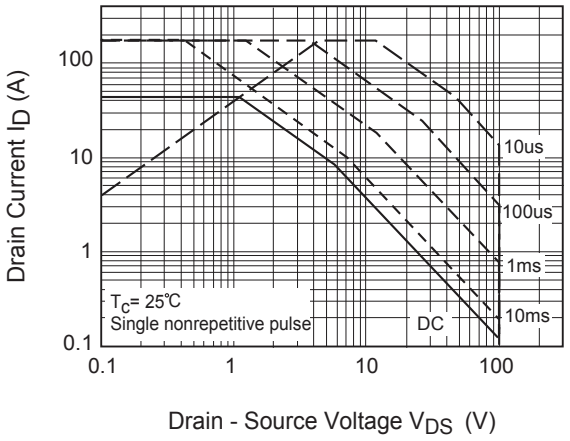


Fig20. Transient Thermal Response Curve
(Junction - Case)

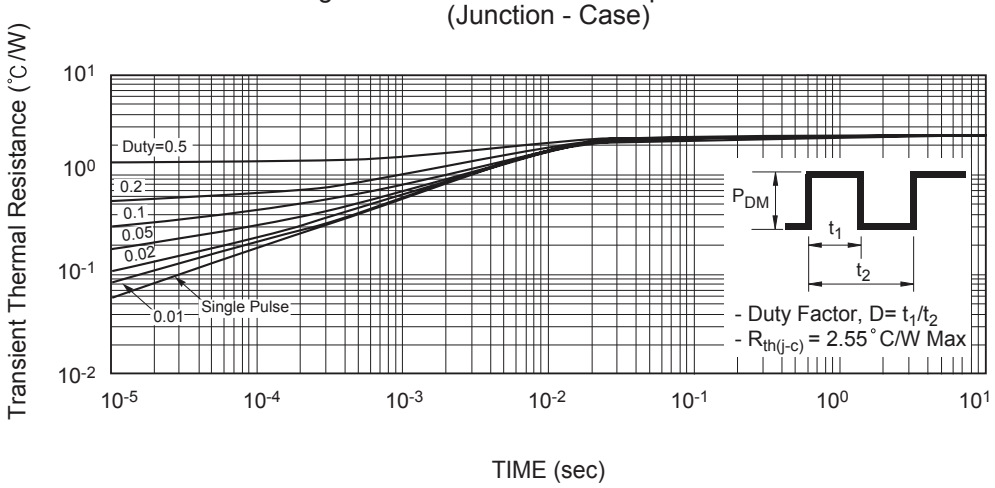


Fig21. Transient Thermal Response Curve
(Junction - Ambient)

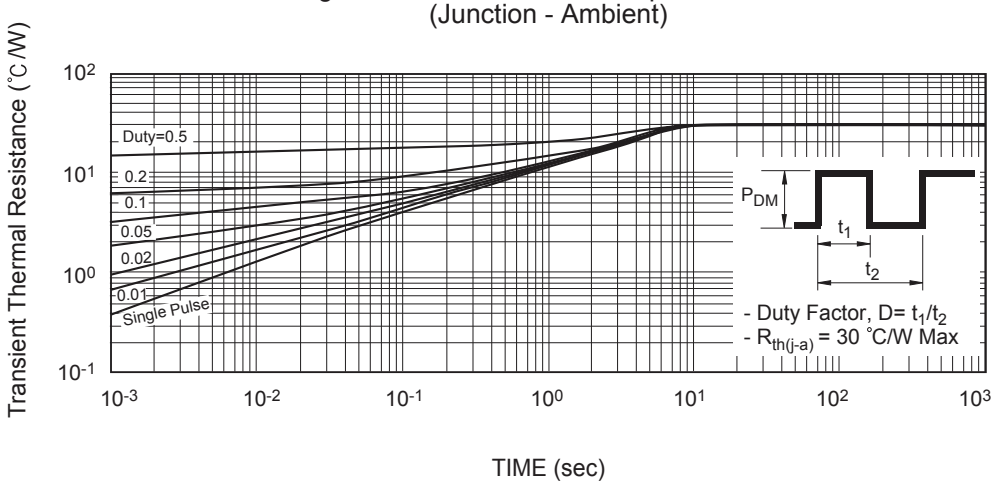
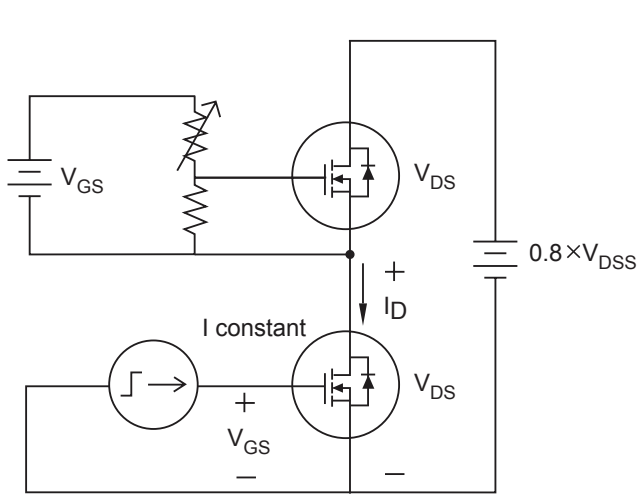


Fig22. Gate Charge



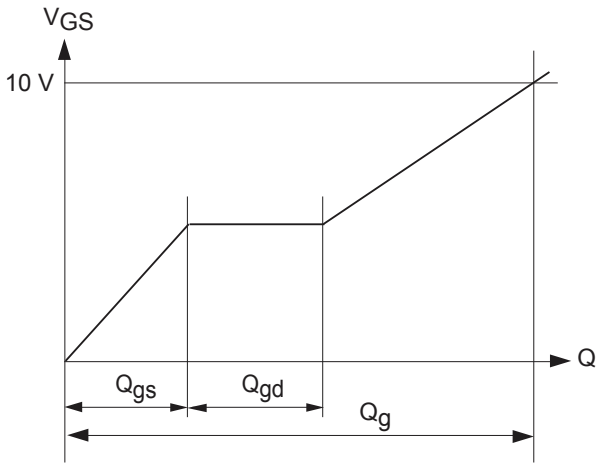
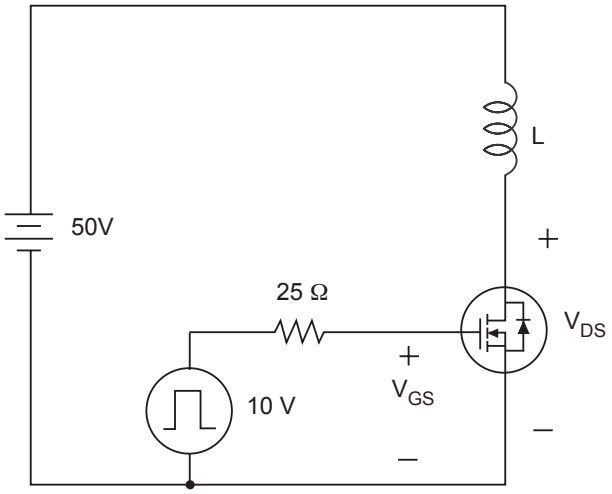


Fig23. Single Pulsed Avalanche Energy



$$E_{AS}=\frac{1}{2}\ LI_{AS}^2\frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$

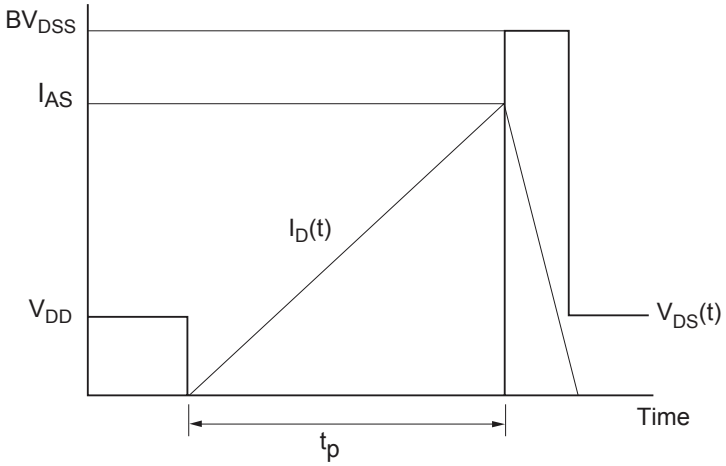
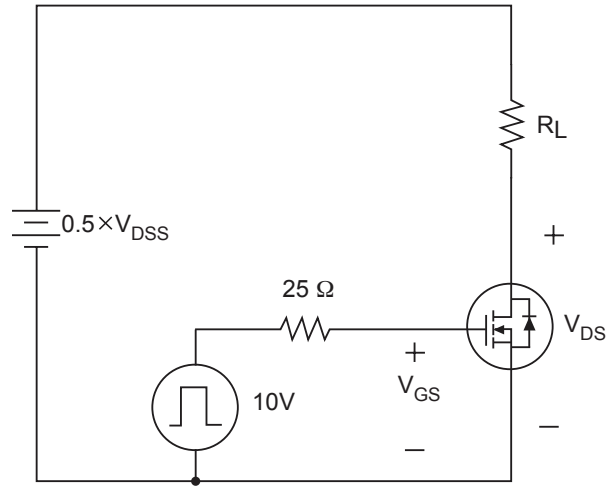


Fig24. Resistive Load Switching



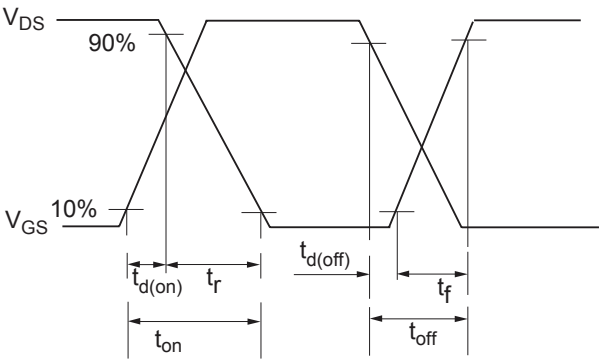
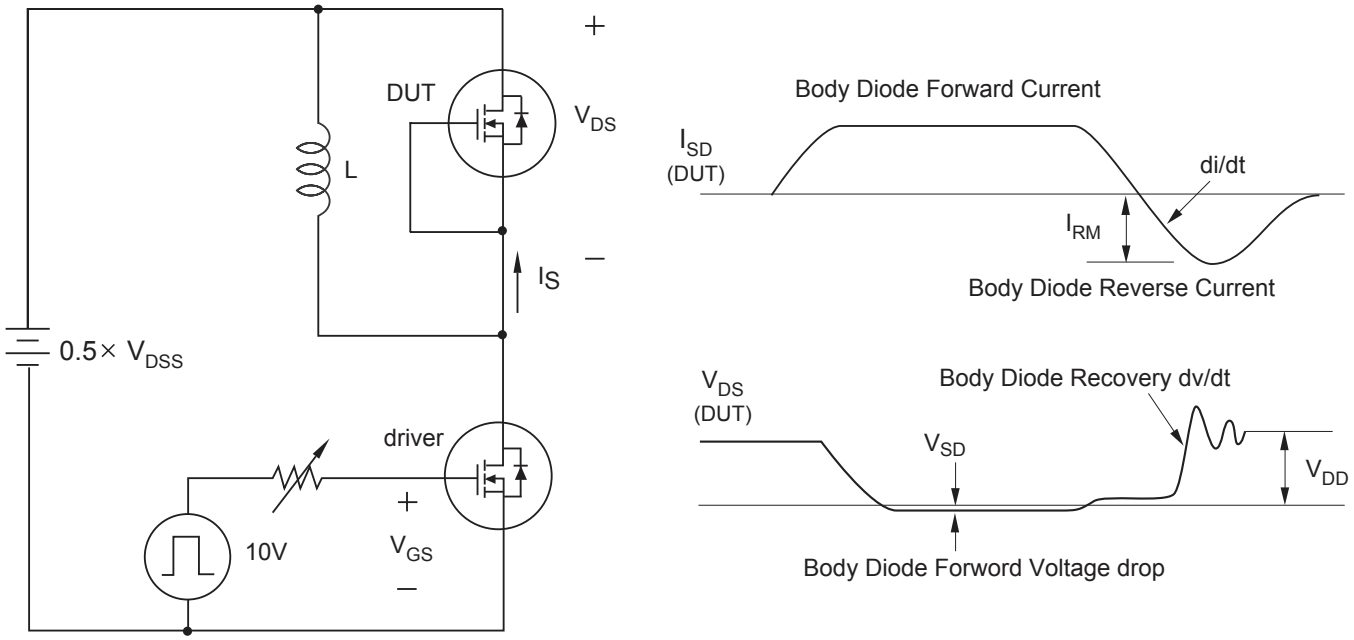
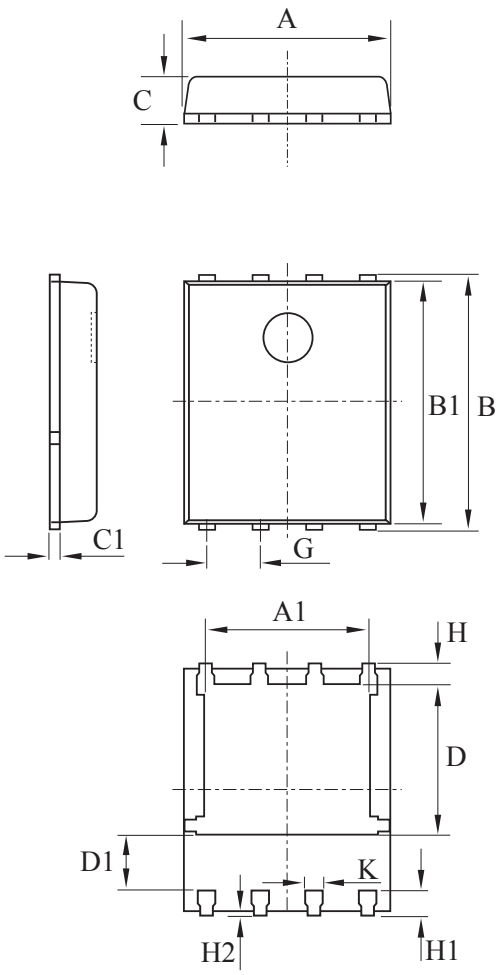


Fig25. Source - Drain Diode Reverse Recovery and dv /dt



PACKAGE OUTLINE

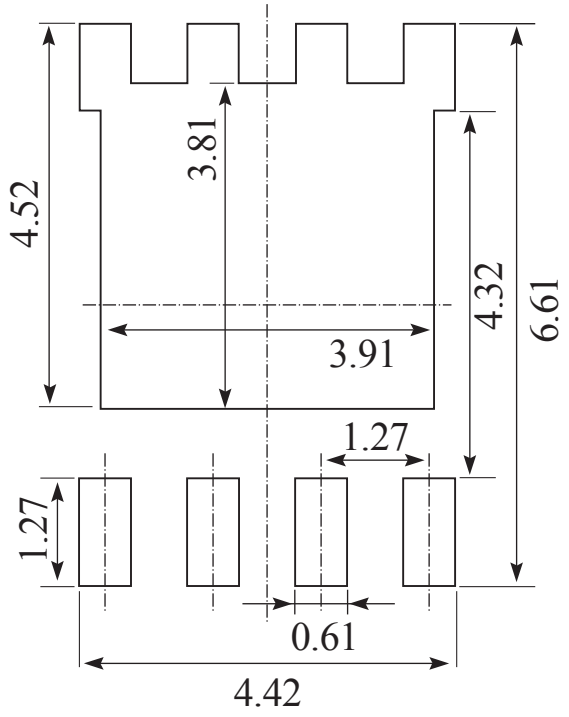


DIM	MILLIMETERS
A	4.9 ± 0.1
A1	3.81+0.15/-0.2
B	6.0 ± 0.1
B1	5.75 ± 0.1
C	1.0 ± 0.1
C1	0.25 ± 0.05
D	3.58 ± 0.20
D1	1.1 Min.
G	1.27 Typ.
H	0.51 ± 0.1
H1	0.61 ± 0.1
H2	0.13 ± 0.07
K	0.41+0.1/-0.08

PDFN56

RECOMMENDED PAD DIMENSION

Unit : mm



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