

General Description

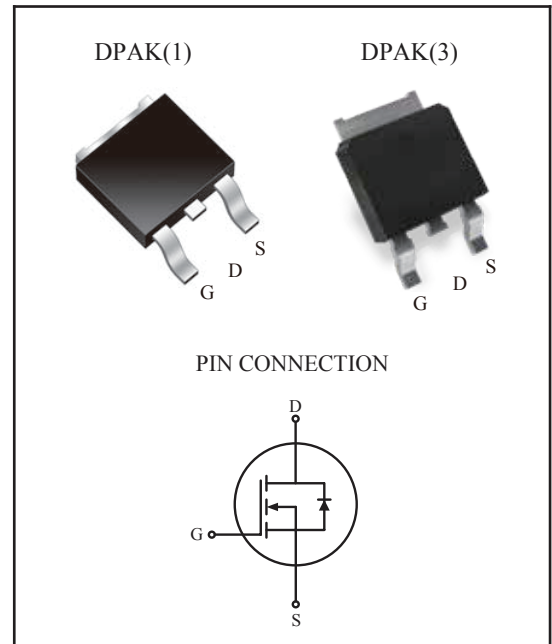
This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for DC/DC Converter, Synchronous Rectification and a load switch in battery powered applications.

FEATURES

- Split Gate Trench Technology
- Ultra low on-resistance
- Ultra Low gate charge (typ. $Q_g=18\text{nC}$)
- Periodic avalanche rated
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC
- Ideal for high-frequency switching and synchronous rectification

MAIN PARAMETER

V_{DS}	100	V
$R_{DS(ON)}$ (Max)@ $V_{GS}=10\text{V}$	22	$\text{m}\Omega$
I_D	32	A

MAXIMUM RATING ($T_j=25^\circ\text{C}$)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	@ $T_C=25^\circ\text{C}$	I_D	32	A
	@ $T_C=100^\circ\text{C}$		20	
	Pulsed (Note 1)	I_{DP}	120*	
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	39	mJ
Repetitive Avalanche Energy (Note 1)		E_{AR}	2.1	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Drain Power Dissipation	@ $T_C=25^\circ\text{C}$	P_D	39	W
	Derate above 25°C		0.31	W/ $^\circ\text{C}$
Maximum Junction Temperature		T_j	150	$^\circ\text{C}$
Storage Temperature Range		T_{stg}	-55 ~ 150	$^\circ\text{C}$
Thermal Characteristics				
Thermal Resistance, Junction-to-Case	@ $T_C=25^\circ\text{C}$	R_{thJC}	3.1	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	@ $T_A=25^\circ\text{C}$	R_{thJA}	110	$^\circ\text{C}/\text{W}$

* : Drain current limited by maximum junction temperature.

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ELECTRICAL CHARACTERISTICS (T_J=25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	100	-	-	V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C	-	0.05	-	V/°C
Drain Cut-off Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V,	-	-	10	μA
Gate Threshold Voltage	V _{th}	V _{DS} =V _{GS} , I _D =250μA	2.0	-	4.0	V
Gate Leakage Current	I _{GSS}	V _{GS} =± 20V, V _{DS} =0V	-	-	± 100	nA
Drain-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =16A	-	17	22	mΩ
Dynamic						
Total Gate Charge	Q _g	V _{DS} =80V, I _D =32A V _{GS} =10V (Note4,5)	-	18	-	nC
Gate-Source Charge	Q _{gs}		-	6.6	-	
Gate-Drain Charge	Q _{gd}		-	5.2	-	
Turn-on Delay time	t _{d(on)}	V _{DD} =50V I _D =32A R _G =25Ω (Note4,5)	-	28	-	ns
Turn-on Rise time	t _r		-	17	-	
Turn-off Delay time	t _{d(off)}		-	37	-	
Turn-off Fall time	t _f		-	14	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	1170	-	pF
Output Capacitance	C _{oss}		-	480	-	
Reverse Transfer Capacitance	C _{rss}		-	41	-	
Source -Drain Diode Ratings						
Continuous Source Current	I _S	V _{GS} <V _{th}	-	-	28	A
Pulsed Source Current	I _{SP}		-	-	112	
Diode Forward Voltage	V _{SD}	I _S =28A, V _{GS} =0V	-	-	1.4	V
Reverse Recovery Time	t _{rr}	I _S =32A, V _{GS} =0V,	-	61	-	ns
Reverse Recovery Charge	Q _{rr}	dI _S /dt=100A/μs	-	0.11	-	μC

Note 1) Repetivity rating : Pulse width limited by junction temperature.

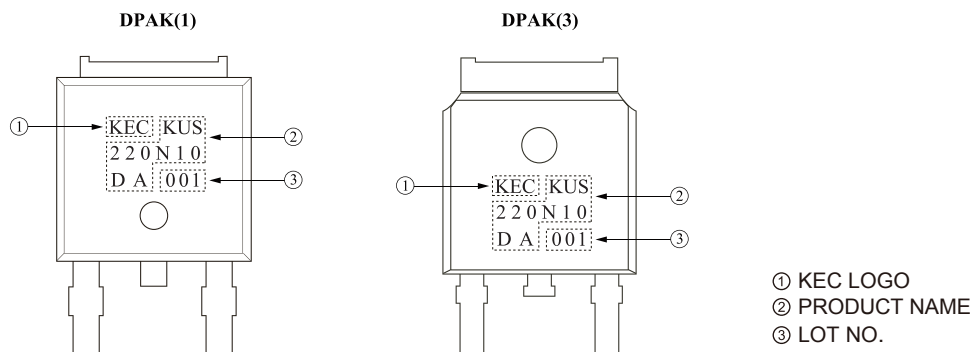
Note 2) L = 43μH, I_S=32A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C.

Note 3) I_S≤ 32A, V_{DD}≤ BV_{DSS}, Starting T_J=25°C.

Note 4) Pulse Test : Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Note 5) Essentially independent of operating temperature.

MARKING



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Fig1. $I_D - V_{DS} - I$

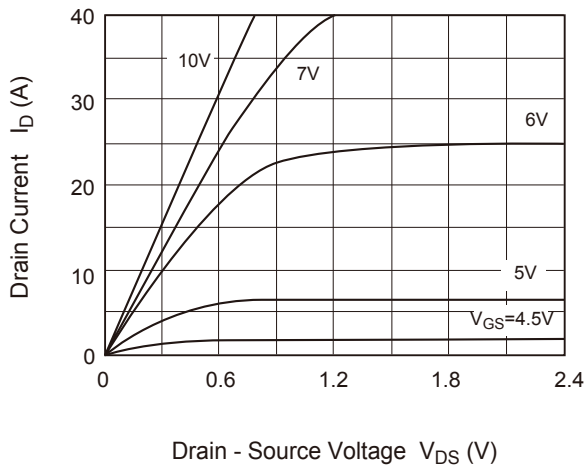


Fig2. $I_D - V_{DS} - II$

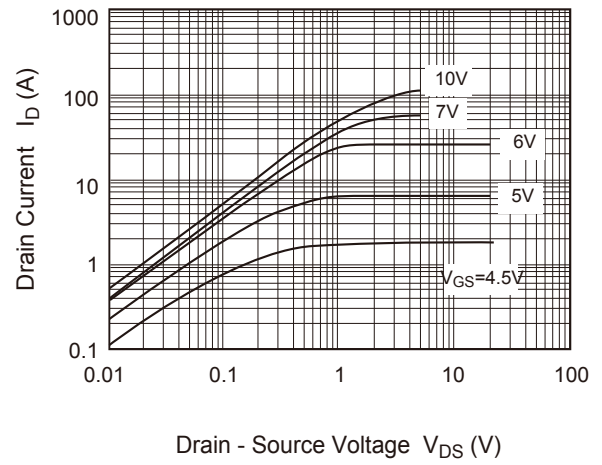


Fig3. $I_D - V_{GS}$

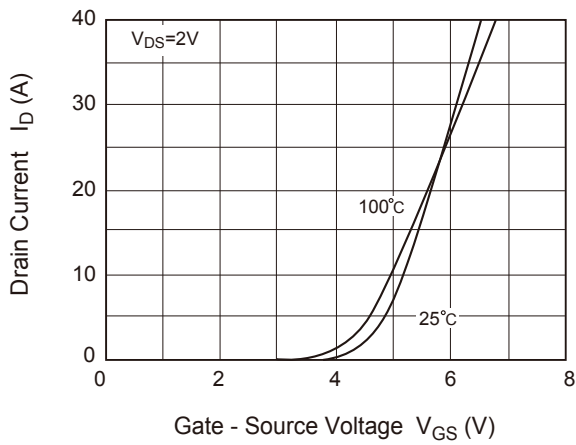


Fig4. $R_{DS(ON)} - I_D$

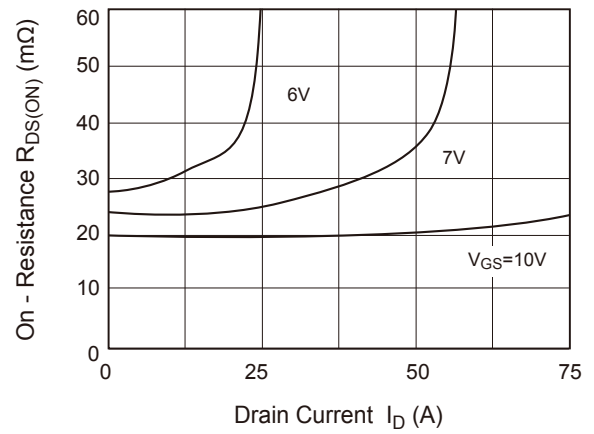


Fig5. $R_{DS(ON)} - V_{GS}$

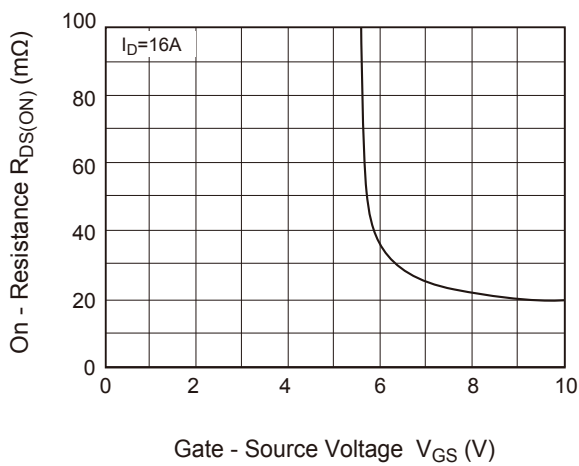
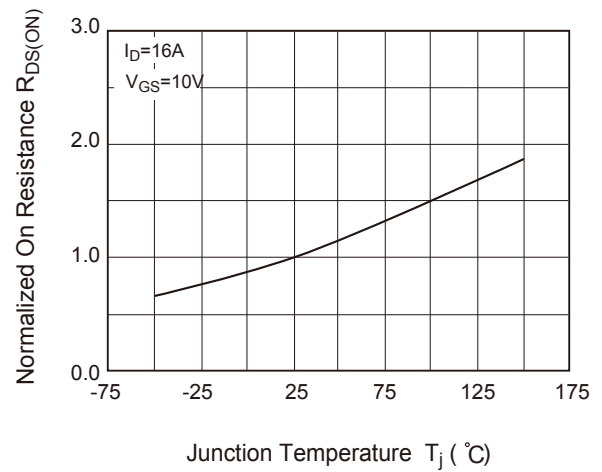


Fig6. $R_{DS(ON)} - T_j$



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Fig7. $BV_{DSS} - T_j$

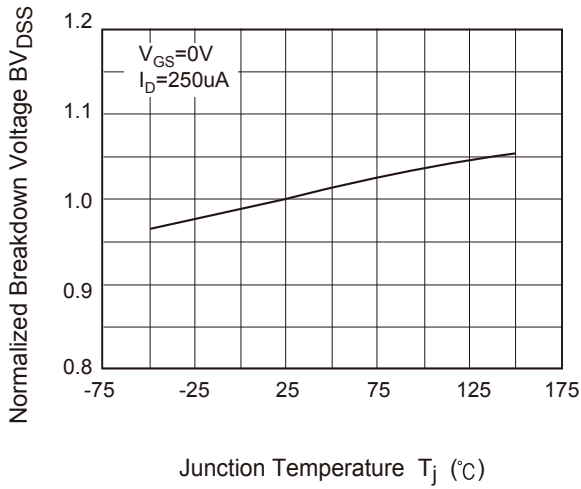


Fig 8. $V_{th} - T_j$

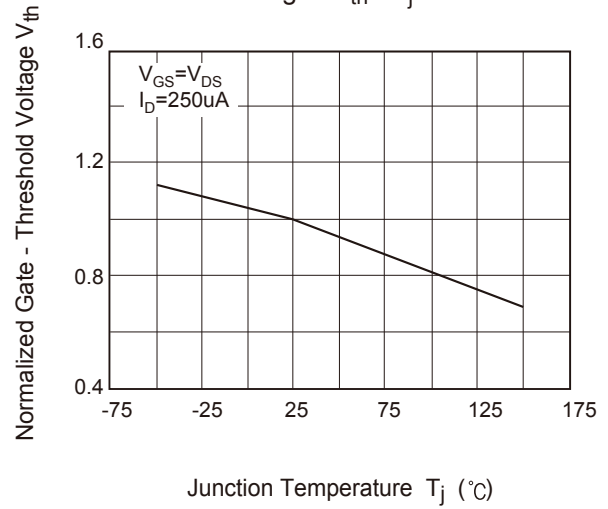


Fig9. $I_S - V_{SD} - I$

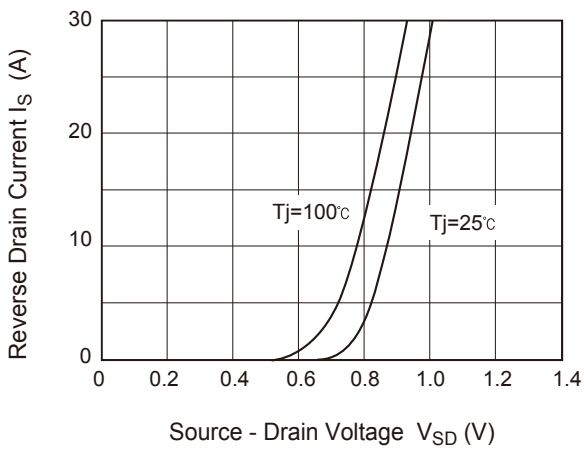


Fig10. $I_S - V_{SD} - II$

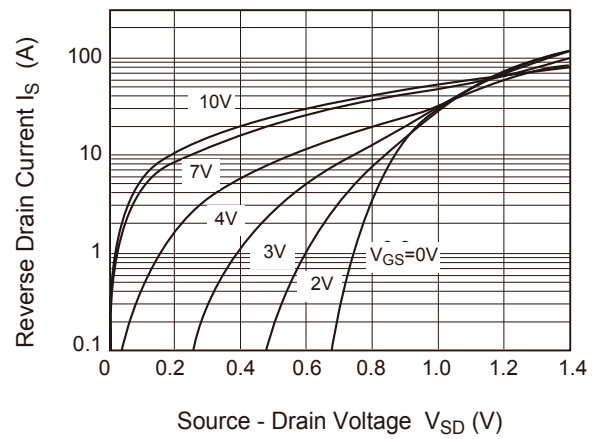


Fig 11. $C - V_{DS}$

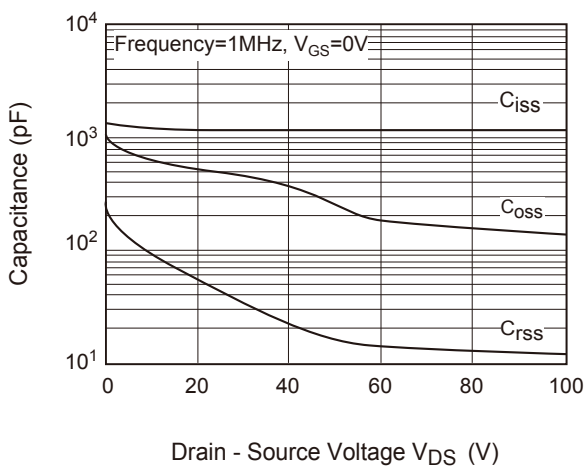
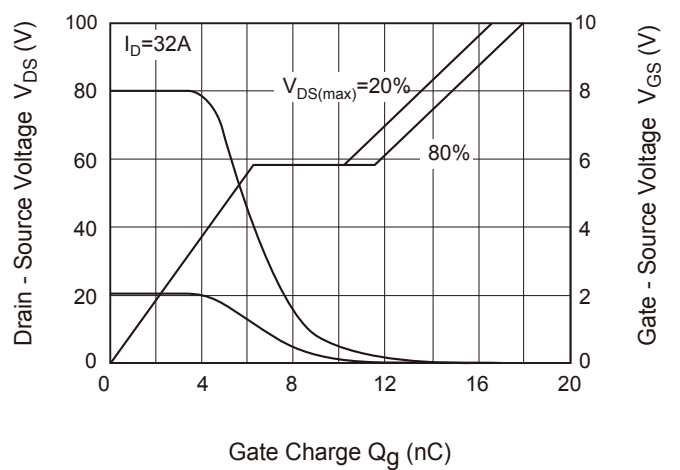


Fig12. $Q_g - V_{DS}$



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Fig13. $I_D - T_j$

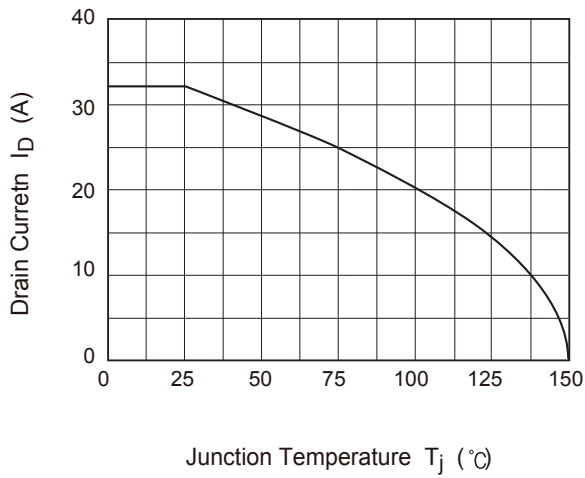


Fig 14. $P_{tot} - T_C$

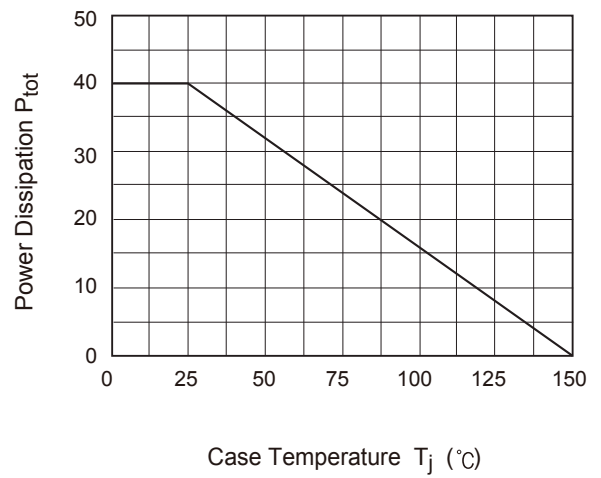


Fig15. S/W Time - I_D

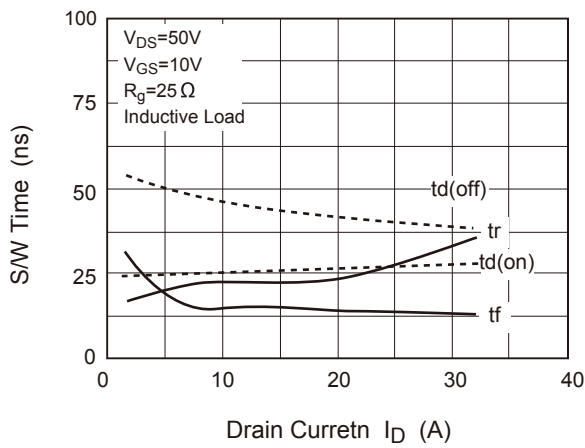


Fig16. S/W Loss - I_D

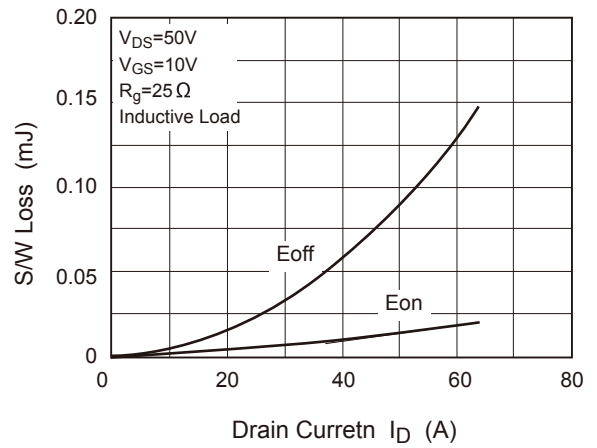


Fig17. S/W Time - R_g

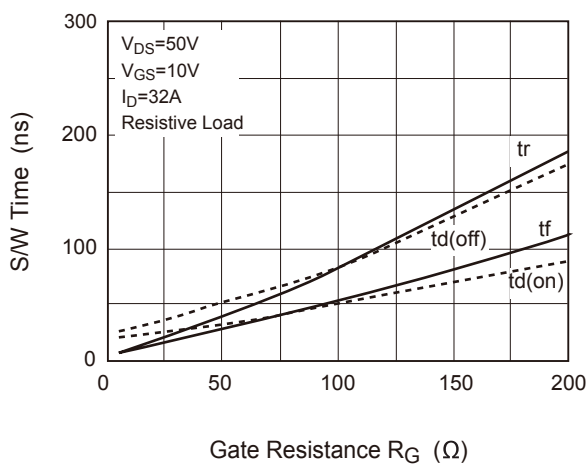
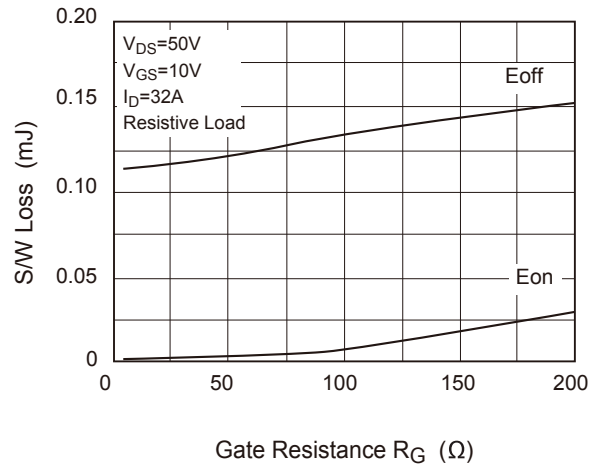


Fig18. S/W Loss - R_g



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Fig 19. Safe Operation Area

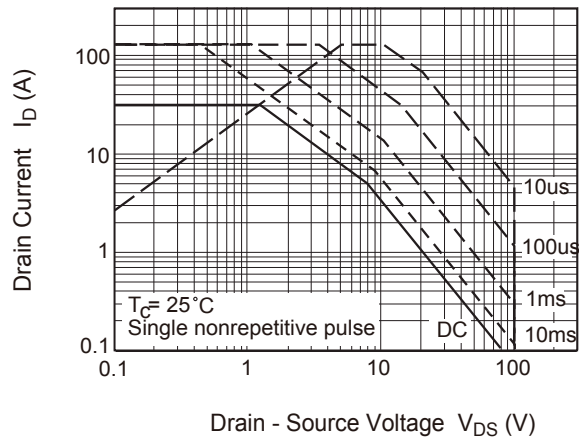


Fig20. Transient Thermal Response Curve
(Junction - Case)

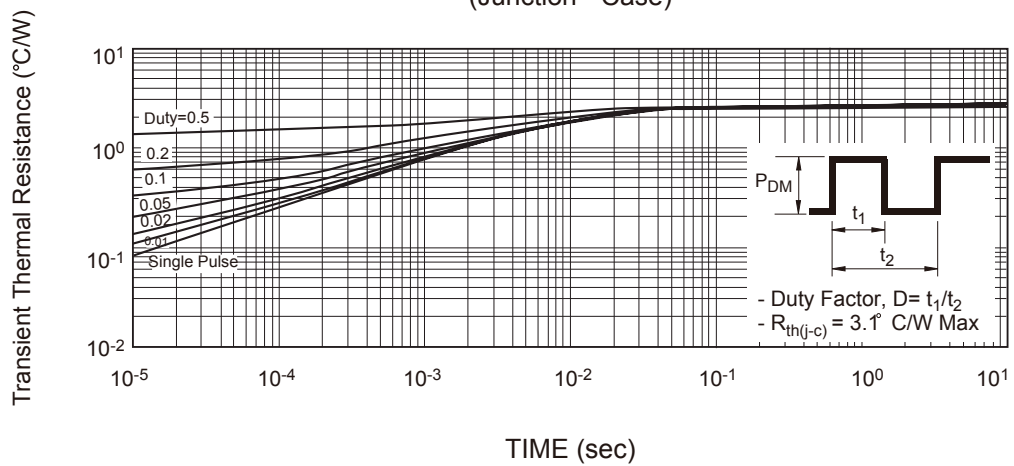


Fig21. Transient Thermal Response Curve
(Junction - Ambient)

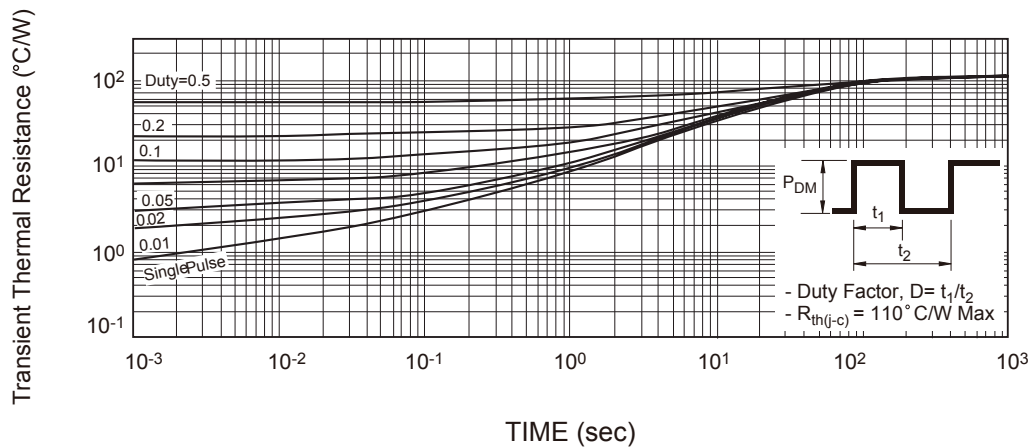


Fig22. Gate Charge

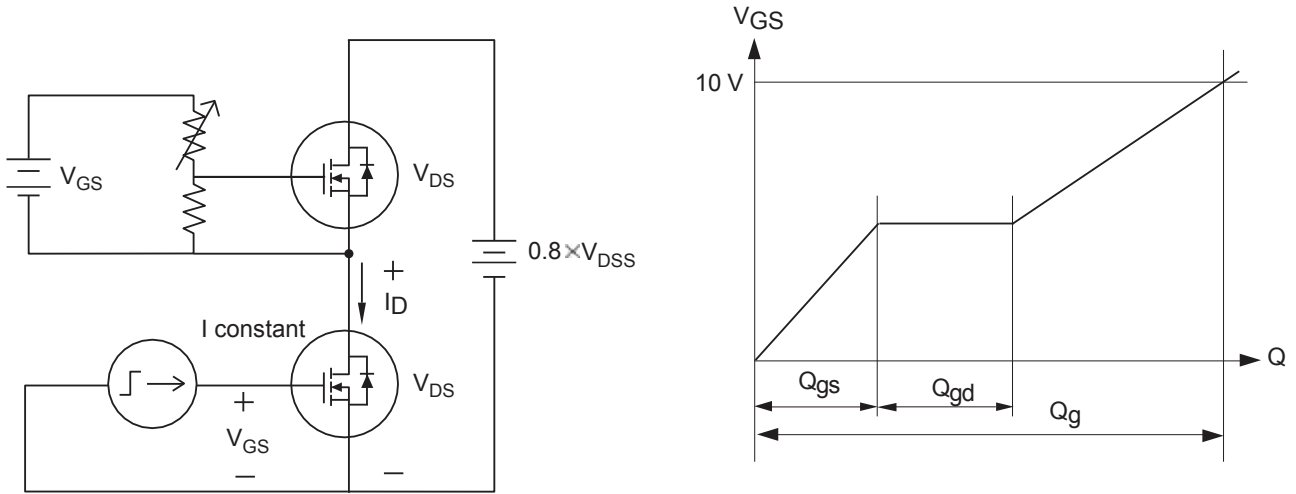


Fig23. Single Pulsed Avalanche Energy

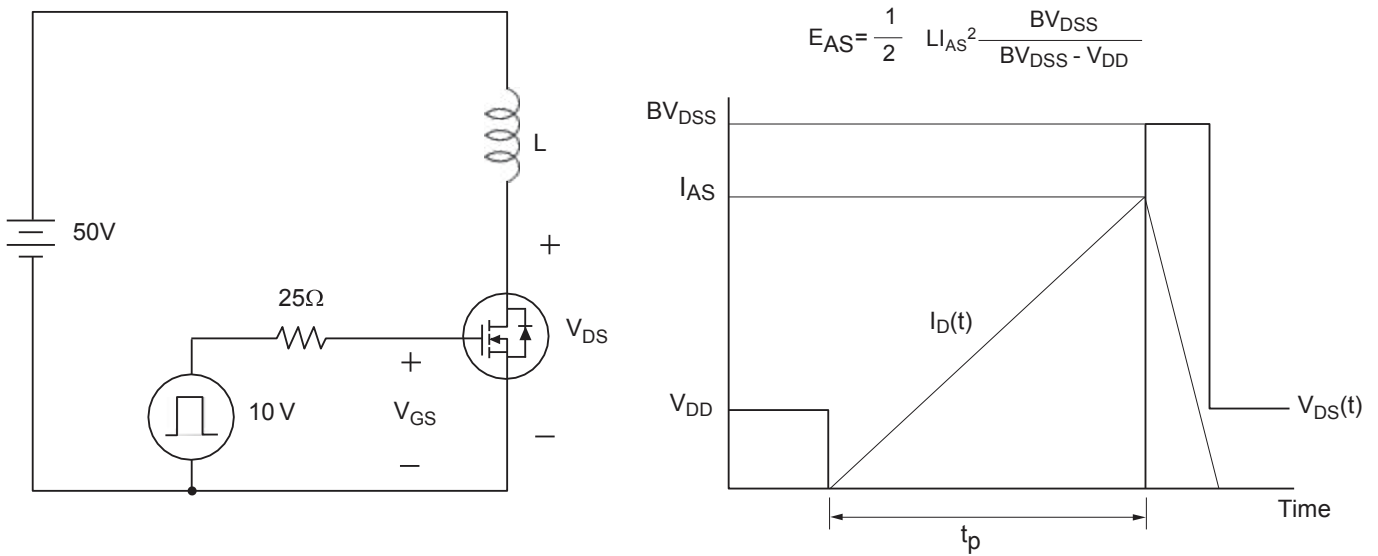


Fig24. Resistive Load Switching

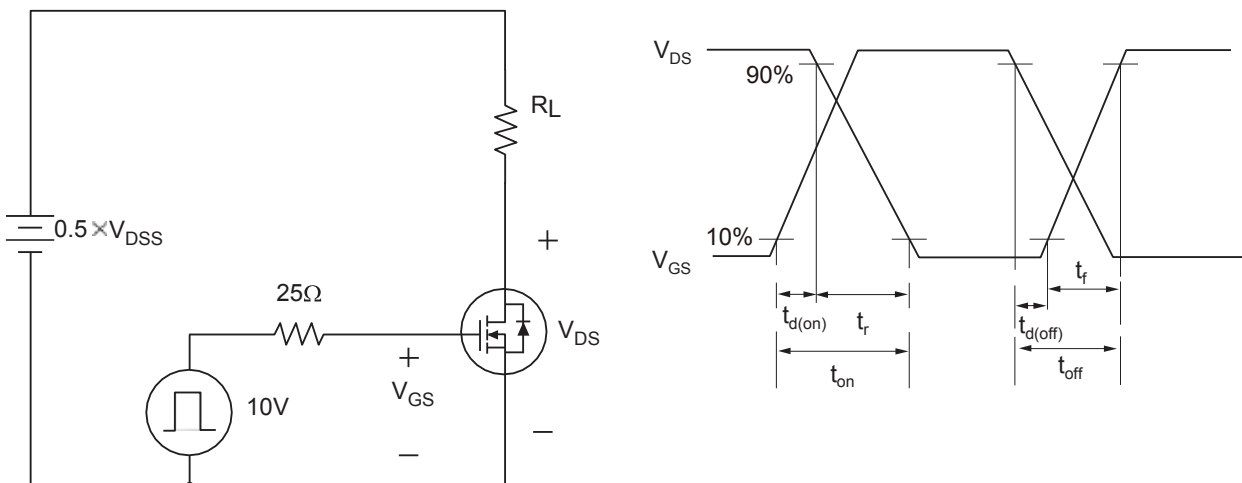
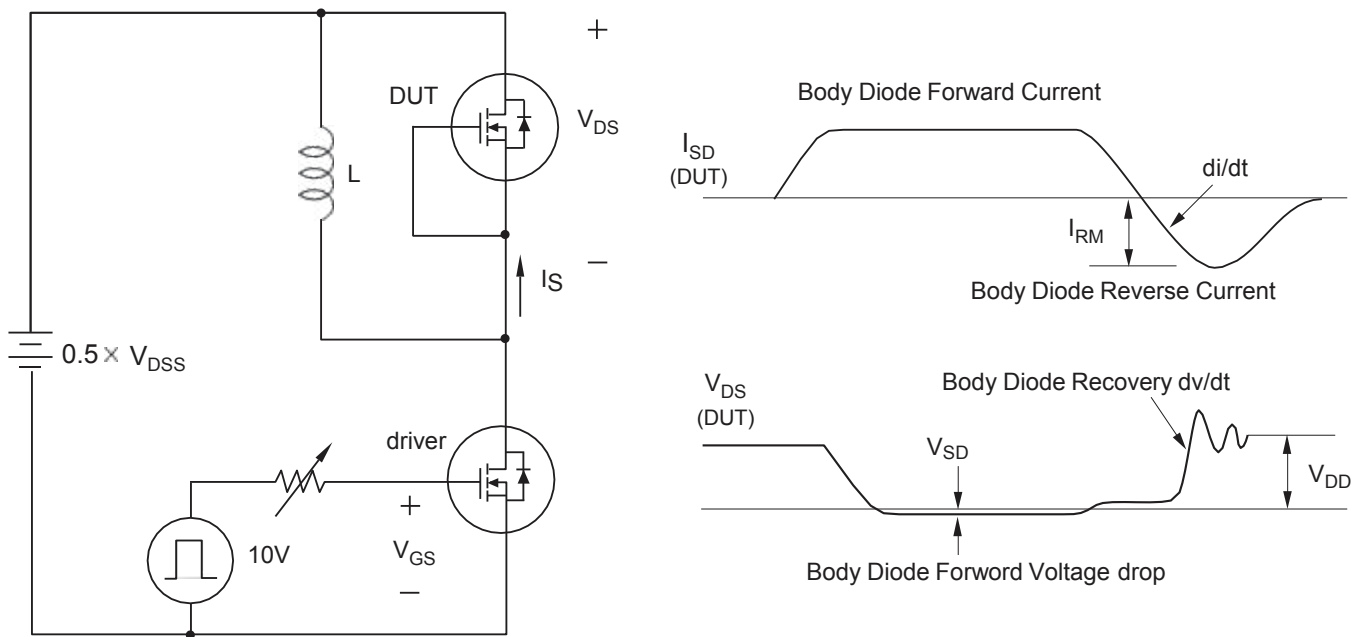


Fig25. Source - Drain Diode Reverse Recovery and dv/dt



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PACKAGE OUTLINE (DPAK(1))

