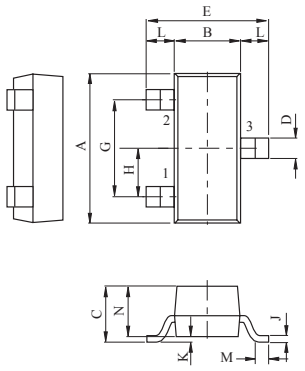
KMD4D2N30S

N-Ch Trench MOSFET

General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for portable equipment.



Unit : mm

DIM	MILLIMETERS
A	2.93 ± 0.20
B	1.30+0.20/-0.15
C	1.0+0.3/-0.1
D	0.40+0.15/-0.05
E	2.40+0.30/-0.20
G	1.90 ± 0.10
H	0.95 ± 0.10
J	0.13+0.10/-0.05
K	0.00 ~ 0.10
L	0.55 ± 0.10
M	0.20 MIN
N	1.00+0.20/-0.10

SOT-23

FEATURES

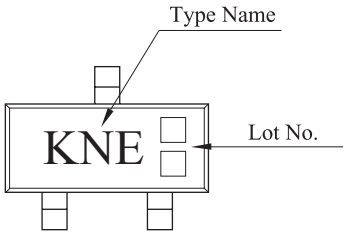
- V_{DSS}=30V, I_D=4.2A
- Drain-Source ON Resistance
  $R_{DS(ON)}$=42mΩ (Max.) @ V_{GS}=10V
  $R_{DS(ON)}$=54mΩ (Max.) @ V_{GS}=4.5V
- Super High Dense Cell Design
- ESD protected

MAXIMUM RATING (Ta=25℃)

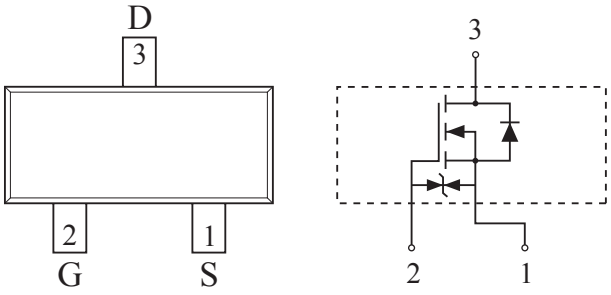
CHARACTERISTIC		SYMBOL	N-Ch	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	DC@T_A=25°C	I_D*	4.2	A
	DC@T_A=70°C		3.3	
	Pulsed	I_{DP}*	20	
Drain-Source-Diode Forward Current		I_S	1.04	A
Drain Power Dissipation	T_A=25°C	P_D*	1.25	W
	T_A=70°C		0.8	
Maximum Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	-55 ~ 150	°C
Thermal Resistance, Junction to Ambient		R_{thJA}*	100	°C/W

Note > *Surface Mounted on 2" x 2" FR4 Board, t ≤ 10sec

Marking



PIN CONNECTION (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_{DS}=250μA, V_{GS}=0V,	30	-	-	V
Drain Cut-off Current	I_{DSS}	V_{GS}=0V, V_{DS}=30V	-	-	0.5	μA
		V_{GS}=0V, V_{DS}=30V, Tj=55°C	-	-	10	
Gate Leakage Current	I_{GSS}	V_{GS}= ± 16V, V_{DS}=0V	-	-	10	μA
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250μA	1.0	-	1.8	V
Drain-Source ON Resistance	$R_{DS(ON)}$*	V_{GS}=10V, I_D=4.2A	-	32	42	mΩ
		V_{GS}=4.5V, I_D=2A	-	40	54	
On-State Drain Current	$I_{D(ON)}$*	V_{GS}=5V, V_{DS}=4.5V	10	-	-	A
Forward Transconductance	g_{fs}*	V_{DS}=5V, I_D=4.2A	-	13	-	S
Dynamic						
Input Capaclitance	C_{iss}	V_{DS}=15V, f=1MHz, V_{GS}=0V	-	310	-	pF
Ouput Capacitance	C_{oss}		-	80	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Total Gate Charge	Q_g* (V_{gs}=10V)	V_{DS}=15V, V_{GS}=10V, I_D=4.2A	-	7.2	-	nC
	Q_g* (V_{gs}=4.5V)		-	3.5	-	
Gate-Source Charge	Q_{gs}*		-	0.8	-	
Gate-Drain Charge	Q_{gd}*		-	1.8	-	
Turn-On Delay Time	$t_{d(on)}$*	V_{DD}=15V, V_{GS}=10V, I_D=4.2A, R_G=6Ω	-	7.0	-	ns
Turn-On Rise Time	t_r*		-	5.3	-	
Turn-Off Delay Time	$t_{d(off)}$*		-	32.0	-	
Turn-Off Fall Time	t_f*		-	3.1	-	
Source-Drain Diode Ratings						
Source-Drain Forward Voltage	V_{SDF}*	V_{GS}=0V, I_{DR}=1A	-	0.8	1.2	V
Reverse Recovery Time	t_{rr}	I_S=4.2A , V_{GS}=0V, dIs/dt=50A/μs	-	24	-	ns
Reverse Recovery Charge	Q_{rr}		-	12	-	nC
NOTE 1> * : Pulse Test : Pulse width <300μs , Duty cycle < 2%						

Fig1. V_{DS} - I_D

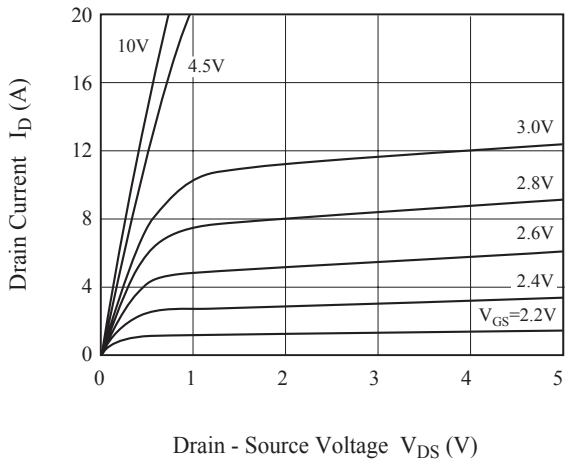


Fig2. $R_{DS(ON)}$ - I_D

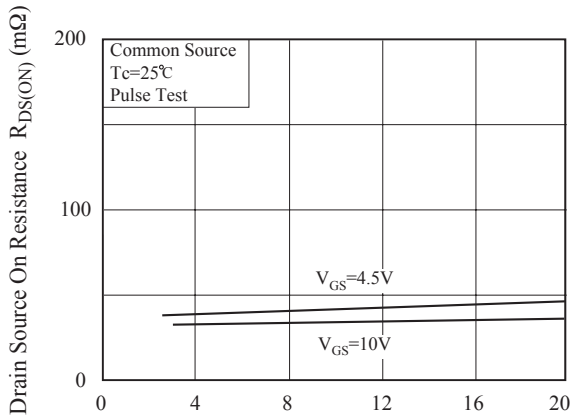


Fig3. I_D - V_{GS}

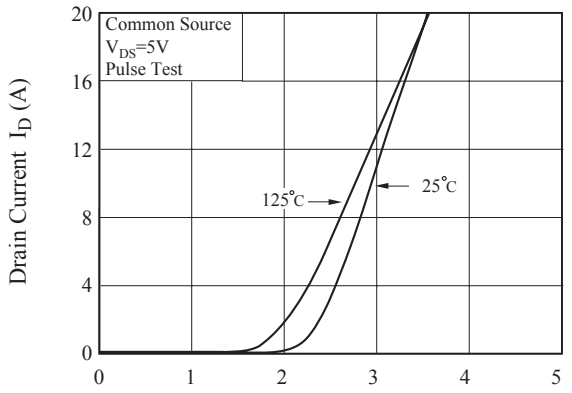


Fig4. $R_{DS(ON)}$ - T_j

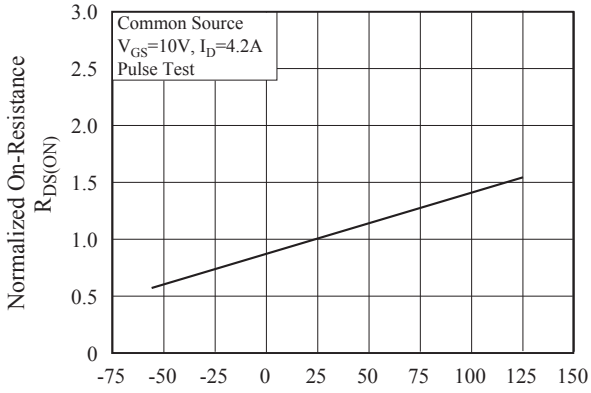


Fig5. V_{th} - T_j

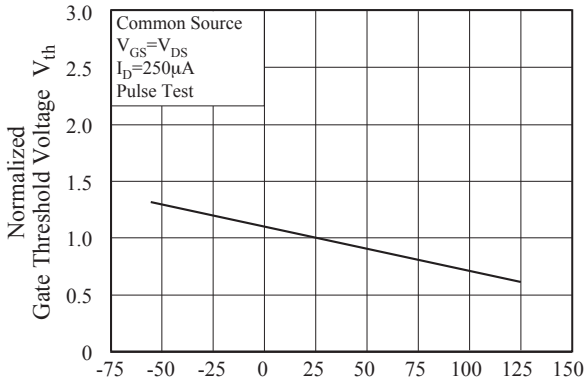


Fig6. I_S - V_{SDF}

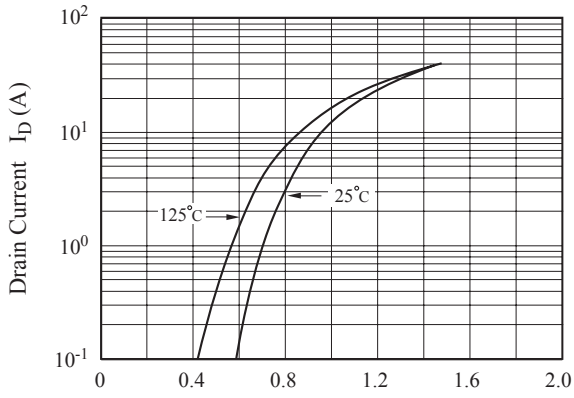


Fig7. Safe Operation Area

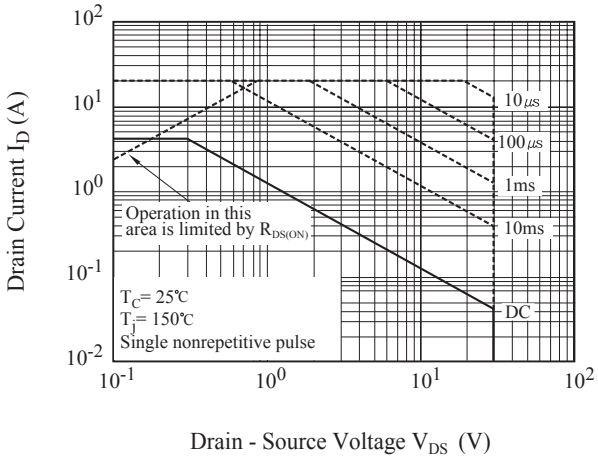


Fig8. Transient Thermal Response Curve

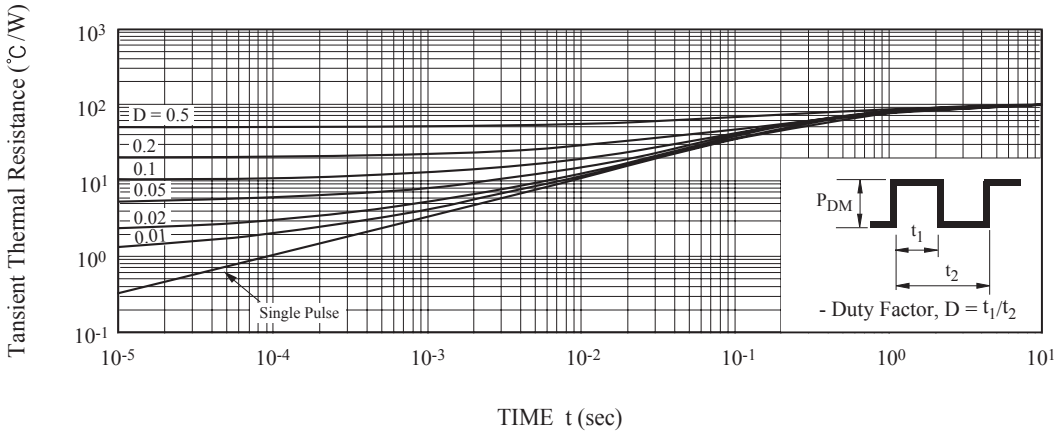


Fig9. Gate Charge Circuit and Wave Form

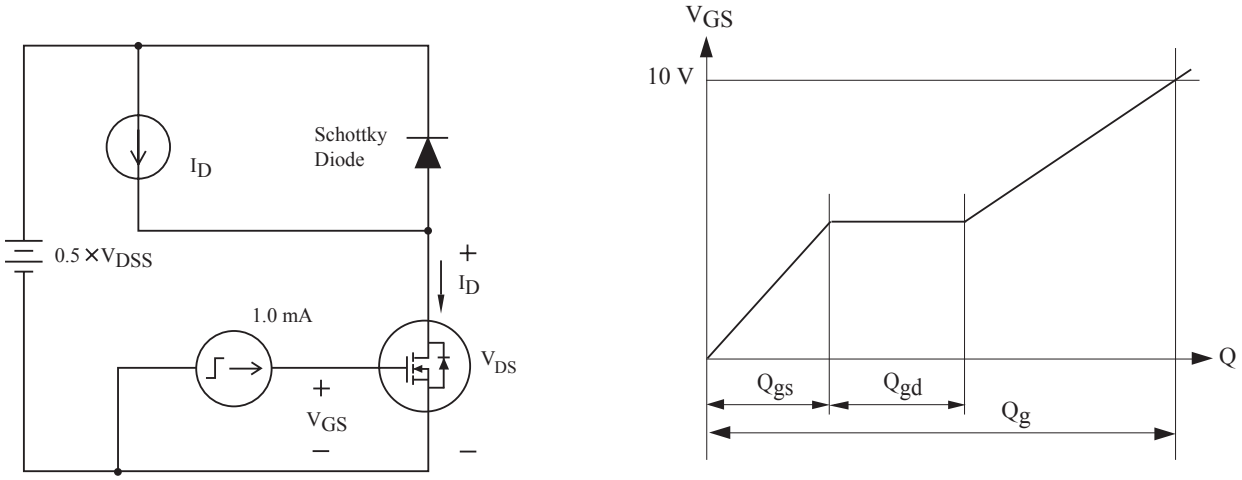


Fig10. Resistive Load Switching

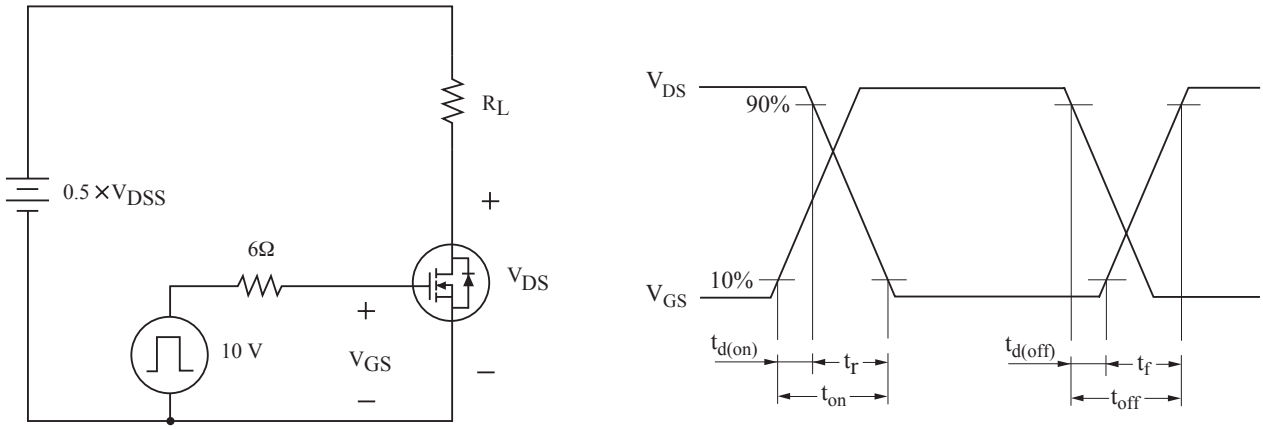


Fig11. Source - Drain Diode Reverse Recovery and dv /dt