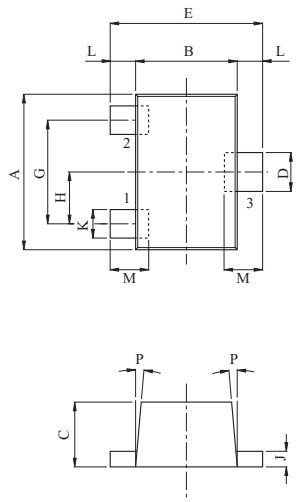
KML0D4N20V

N-Ch Trench MOSFET

General Description

It's mainly suitable for Load Switching Cell Phones, Battery Powered Systems and Level-Shifter.



DIM	MILLIMETERS
A	1.2 ±0.05
B	0.8 ±0.05
C	0.5±0.05
D	0.3±0.05
E	1.2±0.05
G	0.8±0.05
H	0.40
J	0.12±0.05
K	0.2±0.05
L	0.2±0.1
M	0.3±0.1
P	5°

1. Source
2. Gate
3. Drain

VSM

FEATURES

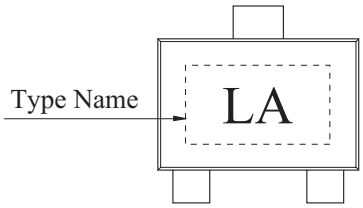
- V_{DSS}=20V, I_D=0.4A.
- Drain-Source ON Resistance .
  : $R_{DS(ON)}$=0.70Ω @ V_{GS}=4.5V
  : $R_{DS(ON)}$=0.85Ω @ V_{GS}=2.5V
  : $R_{DS(ON)}$=1.25Ω @ V_{GS}=1.8V
- Super High Dense Cell Design.
- Suffix U : Qualified to AEC-Q101.
  ex) KML0D4N20V-RTK/HU

MAXIMUM RATING (Ta=25℃)

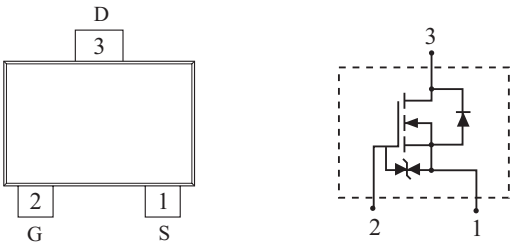
CHARACTERISTIC		SYMBOL	N-Ch	UNIT
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±6	V
Drain Current	DC @T_A=25℃	I_D*	400	mA
	DC @T_A=85℃		280	
	Pulsed	I_{DP}	650	
Source-Drain Diode Current		I_S	125	
Drain Power Dissipation		P_D*	150	mW
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55 150	℃

Note 1) *Surface Mounted on 1□×1□ FR4 Board. t≤5 sec

Marking



PIN CONNECTION (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA, V_{GS}=0V	20	-	-	V
Drain Cut-off Current	I_{DSS}	V_{GS}=0V, V_{DS}=16V	-	0.3	100	nA
Gate Leakage Current	I_{GSS}	V_{GS}=±4.5V, V_{DS}=0V	-	±0.5	±1.0	μA
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250 μA	0.45	-	1.0	V
Drain-Source ON Resistance	$R_{DS(ON)}$*	V_{GS}=4.5V, I_D=400mA	-	0.41	0.70	Ω
		V_{GS}=2.5V, I_D=350mA	-	0.53	0.85	
		V_{GS}=1.8V, I_D=300mA	-	0.70	1.25	
Forward Transconductance	g_{fs}*	V_{DS}=10V, I_D=400mA	-	1.0	-	S
Source-Drain Diode Forward Voltage	V_{SD}*	I_S=150mA, V_{GS}=0V	-	0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g*	V_{DS}=10V, I_D=250mA, V_{GS}=4.5V	-	750	-	pC
Gate-Source Charge	Q_{gs}*		-	75	-	
Gate-Drain Charge	Q_{gd}*		-	225	-	
Turn-on Delay time	$t_{d(on)}$*	V_{DD}=10V, I_D=200mA, V_{GS}=4.5V, R_G=10Ω	-	5	-	ns
Turn-off Delay time	$t_{d(off)}$*		-	25	-	

Note 2) *Pulse test : Pulse width≤300μs, Duty Cycle≤2%.

Fig 1. I_D - V_{DS}

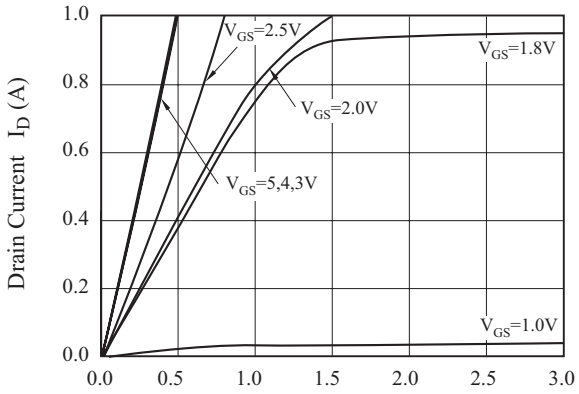


Fig 2. $R_{DS(on)}$ - I_D

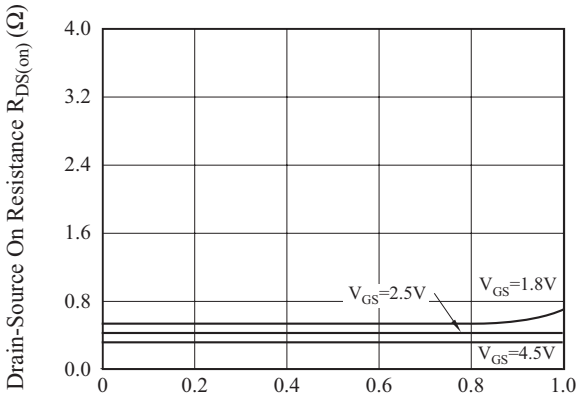


Fig 3. I_D - V_{GS}

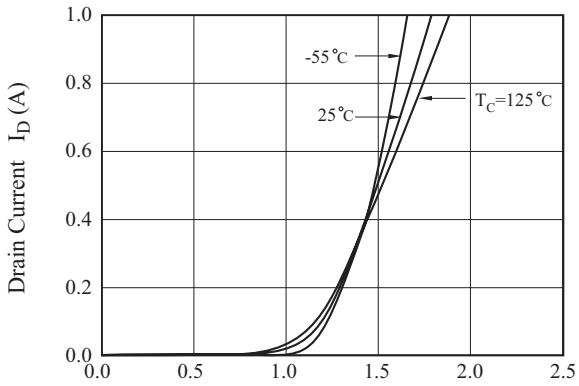


Fig 4. $R_{DS(ON)}$ - T_j

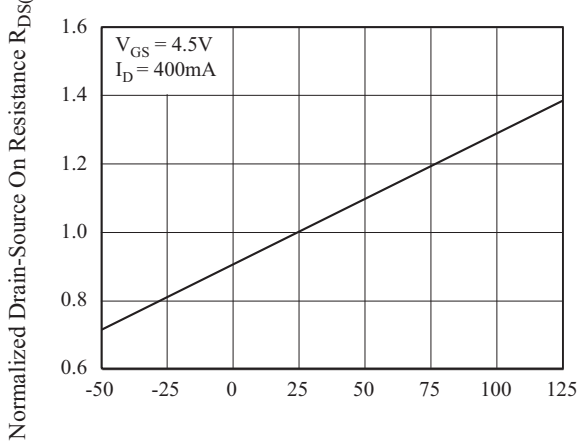


Fig 5. V_{th} - T_j

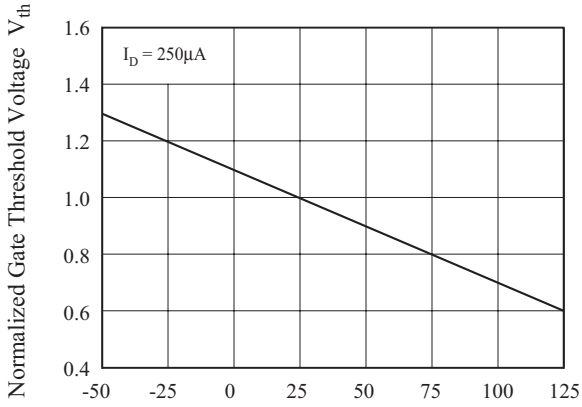


Fig 6. I_{DR} - V_{SDF}

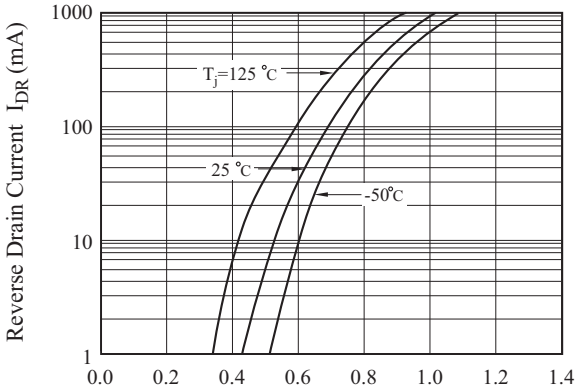


Fig 7. V_{GS} - Q_g

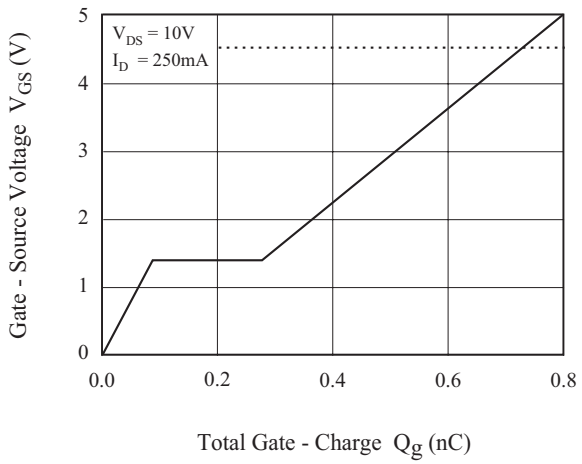


Fig 8. C - V_{DS}

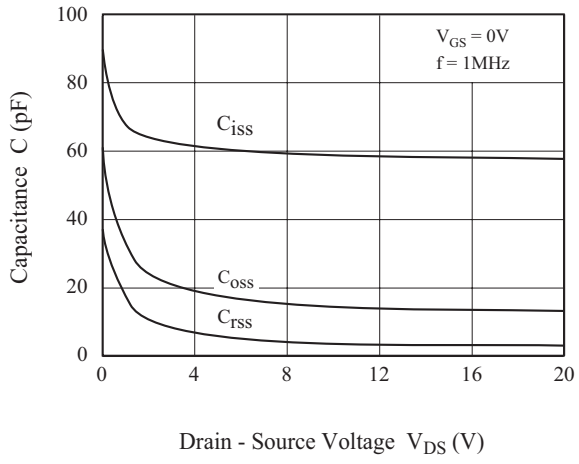


Fig 9. Transient Thermal Response Curve